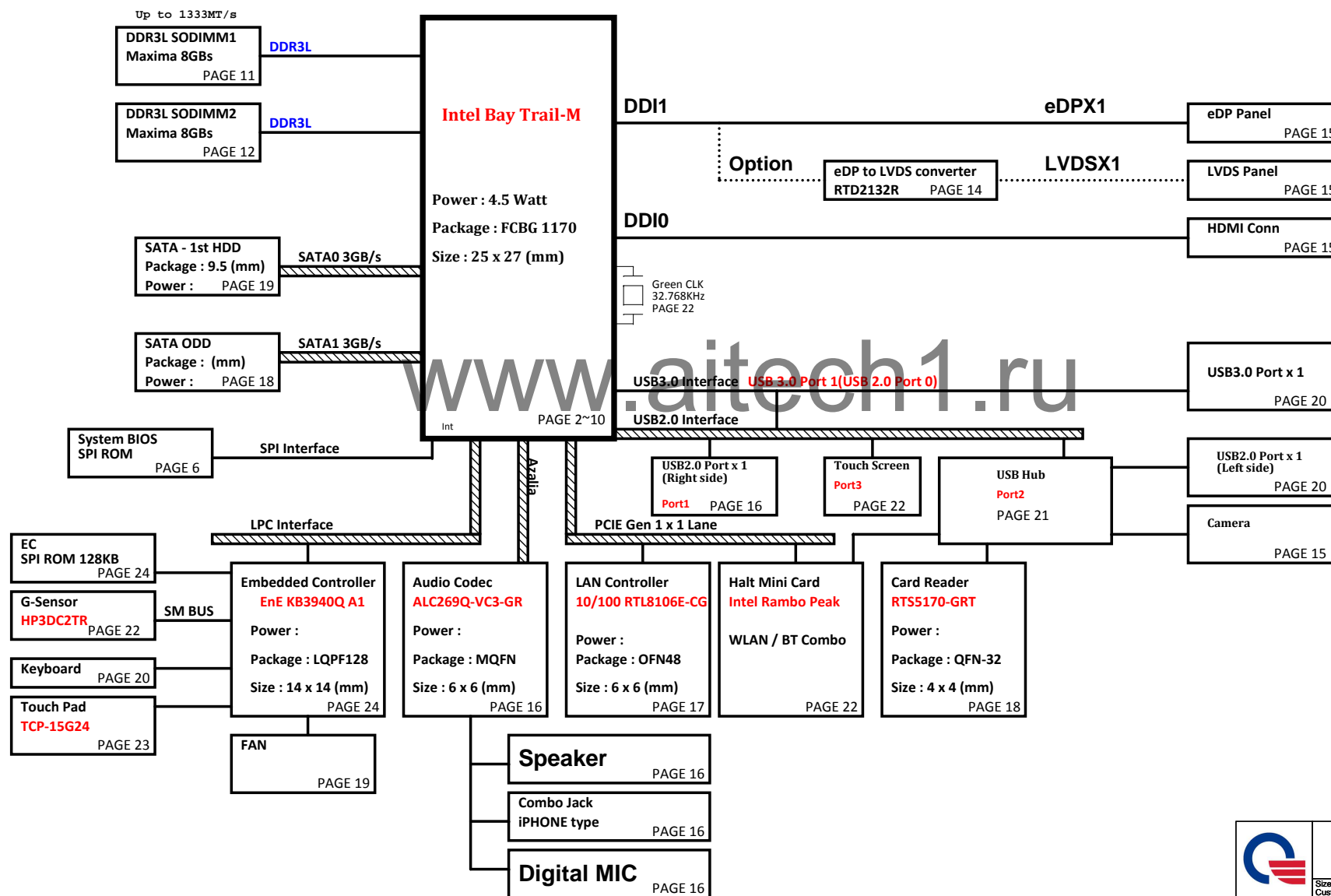


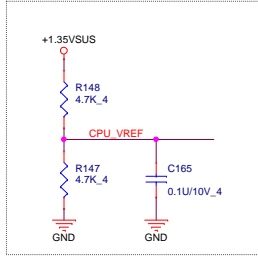
JWM UMA(14")

Intel Bay Trail-M Platform Block Diagram

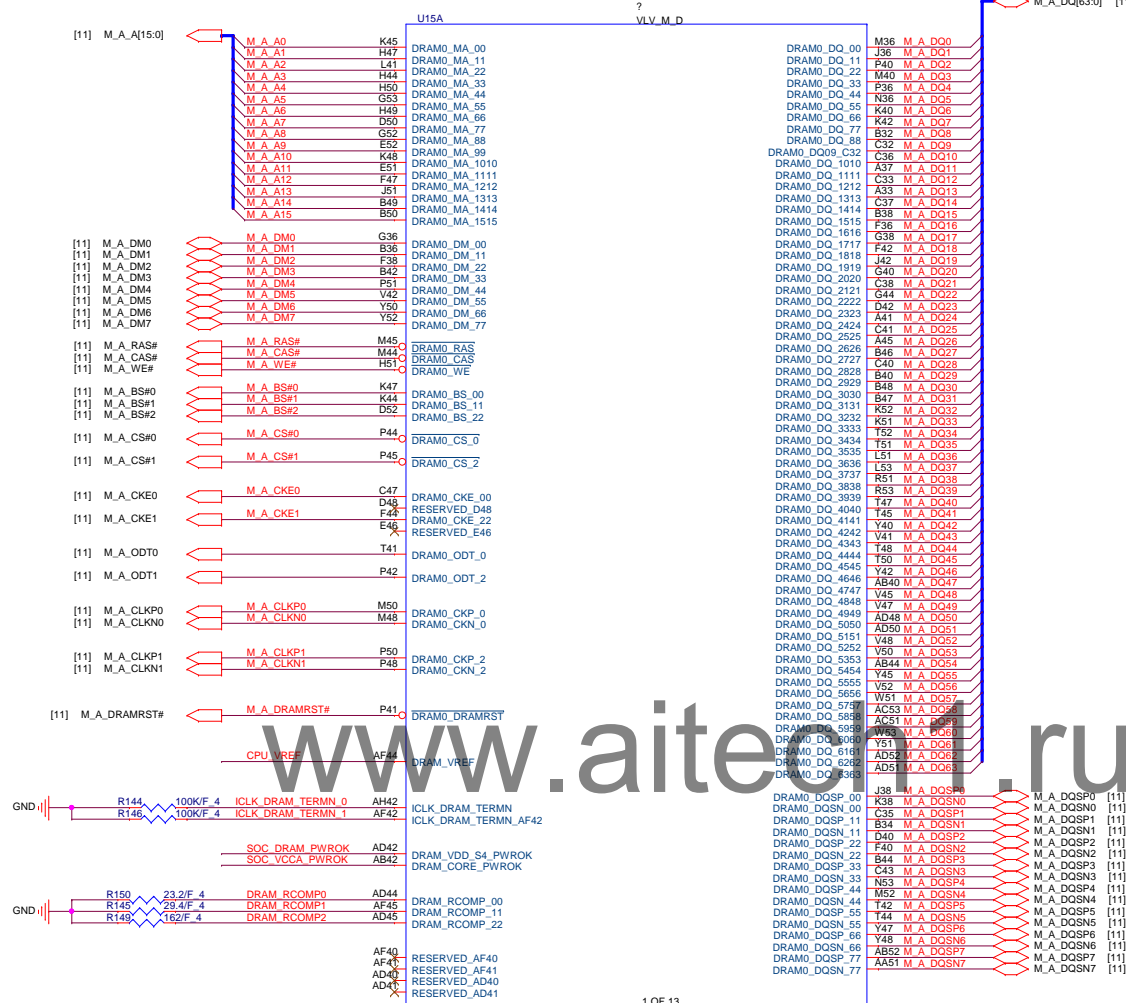
PCB 6L STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(Low)
 LAYER 5 : SVCC
 LAYER 6 : BOT

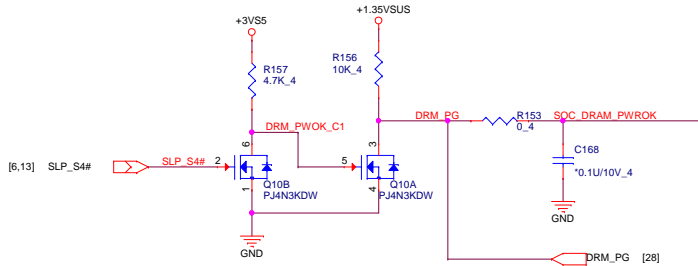




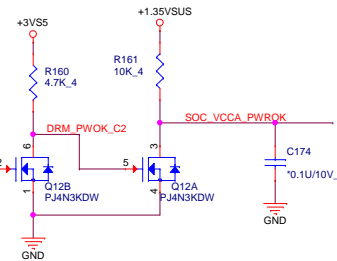
Note: PLACE TWO 4.7K RESISTORS
CLOSE TO CPU PINS ON M_VREF



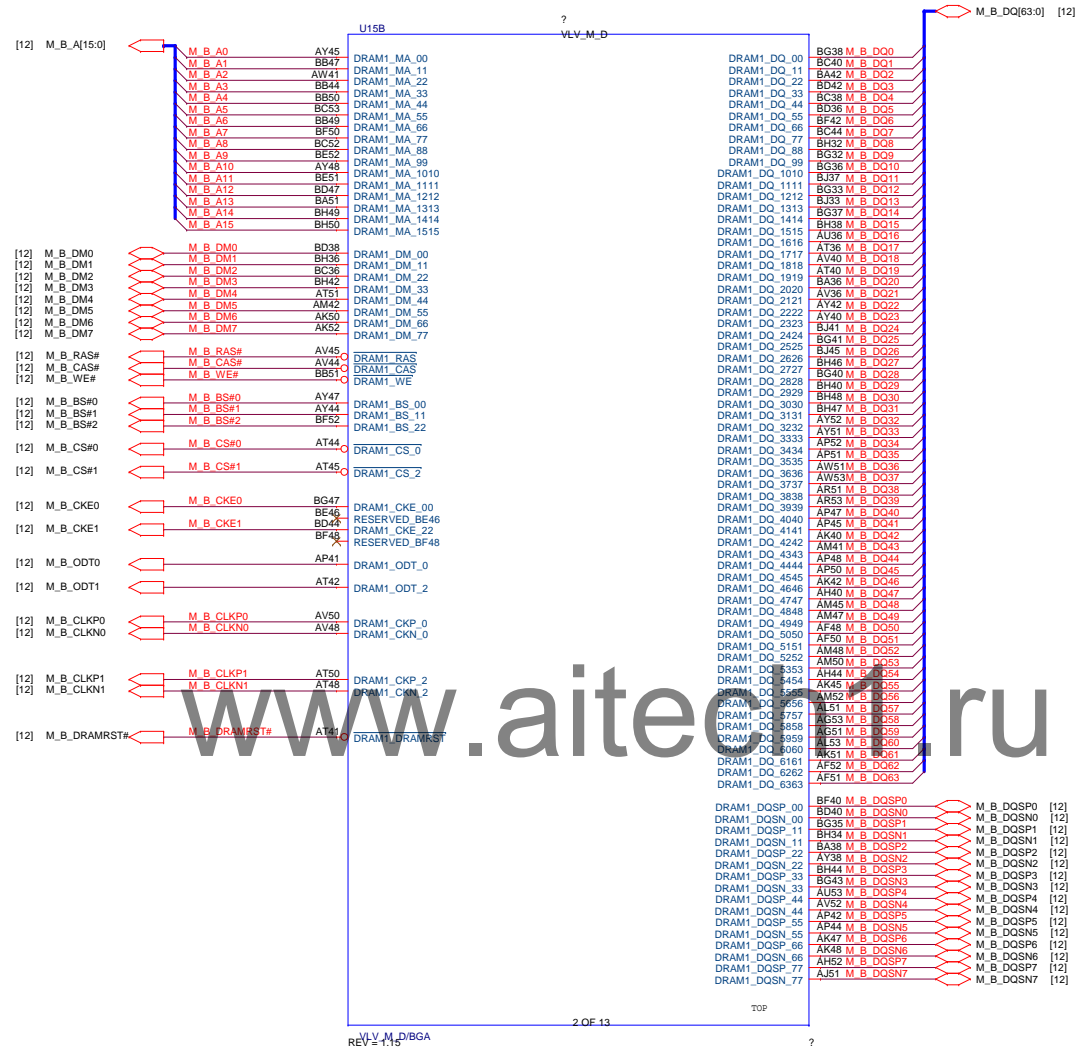
VLV_M_D/BGA ph
REV = 1.15
0624 @ALF:
Changed to QCI P/N for JWM



[13,24] EC_PWROK

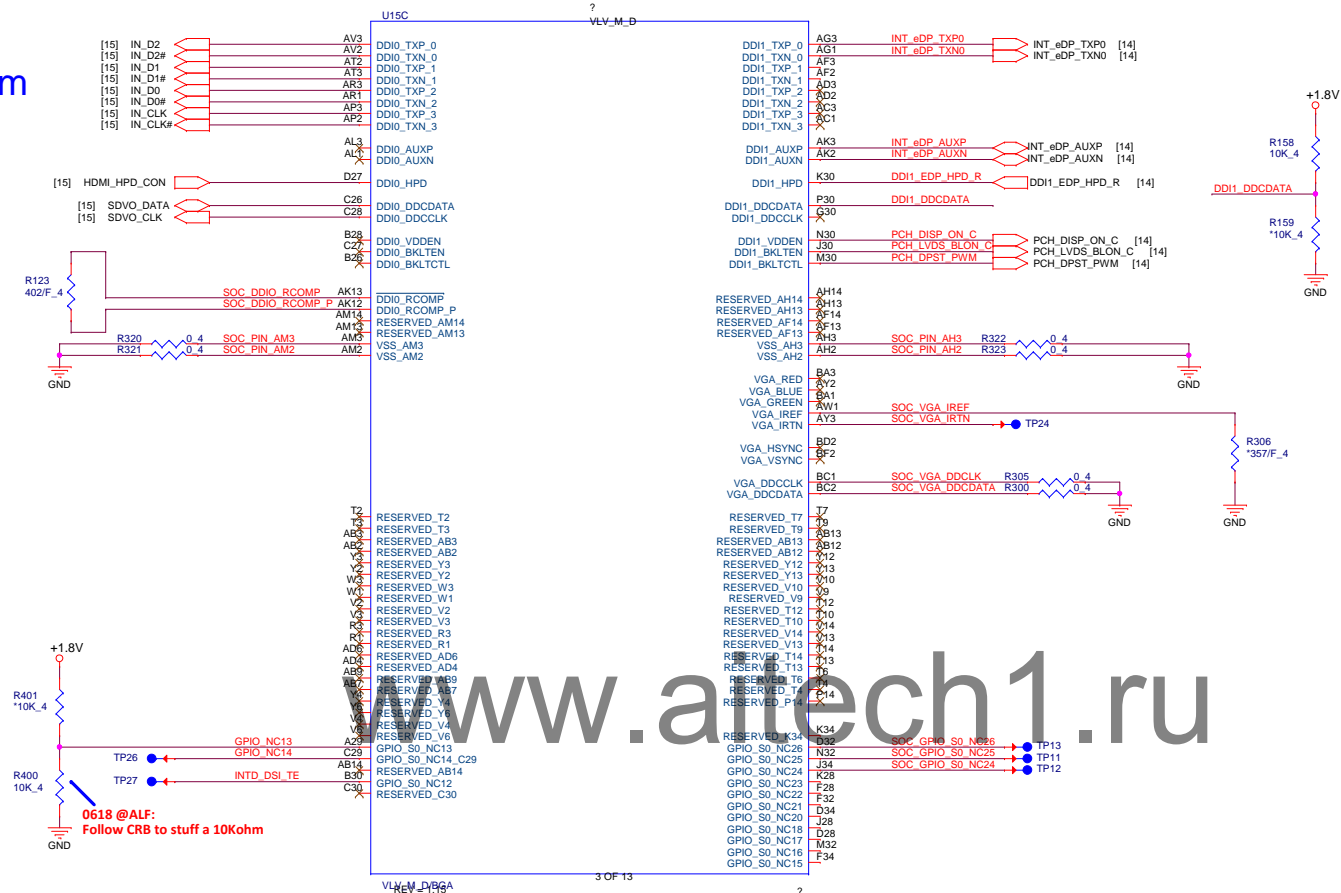


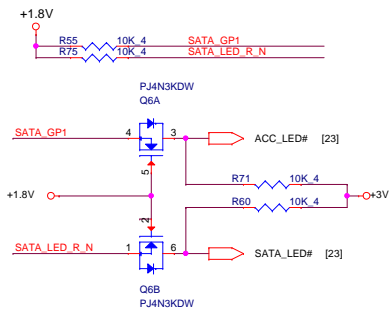
www.qdzbwx.com



PROJECT :JWM
Quanta Computer Inc.

Size Custom	Document Number Valley 2/9 (DDR)	Rev 1A
Date: Tuesday, August 20, 2013		Sheet 3 of 39



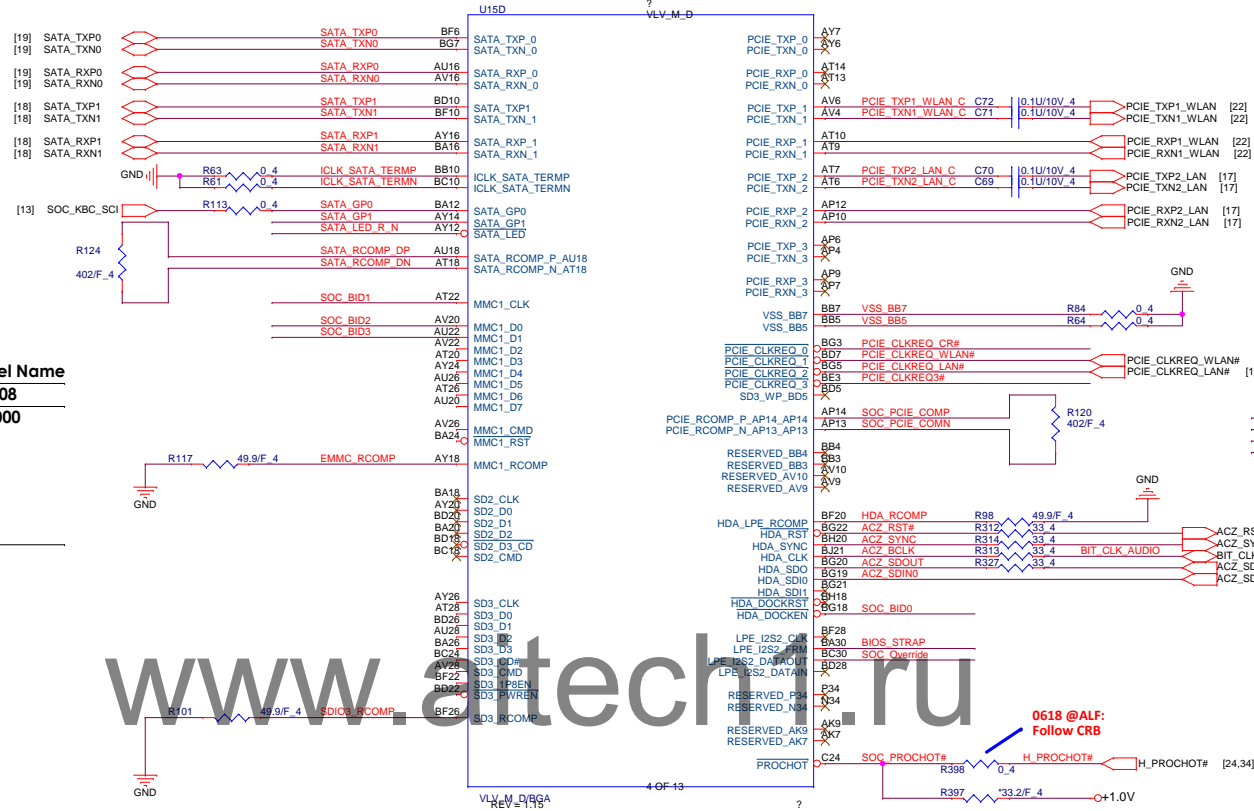
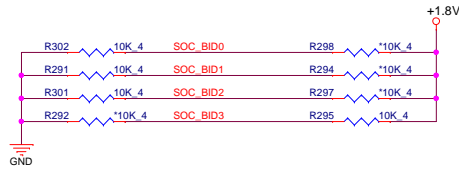


JWM BOARD ID SETTING

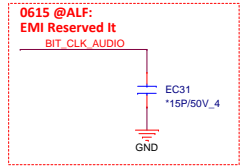
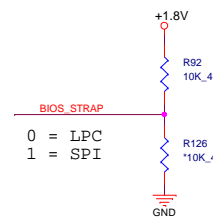
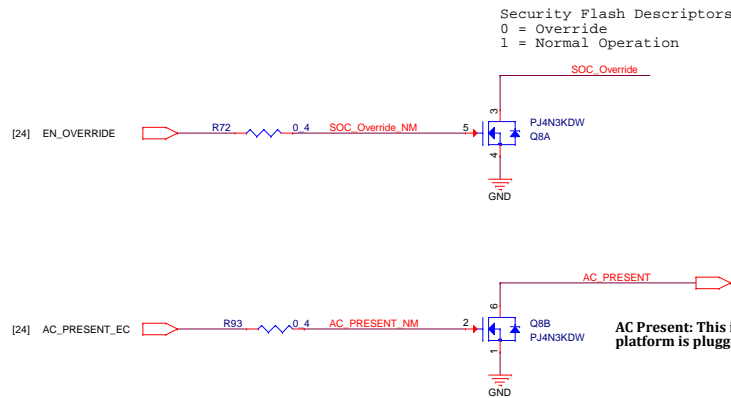
GPIO_SO_SC[015]	SOC_BID0	BIT0
GPIO_SO_SC[016]	SOC_BID1	BIT1
GPIO_SO_SC[017]	SOC_BID2	BIT2
GPIO_SO_SC[018]	SOC_BID3	BIT3

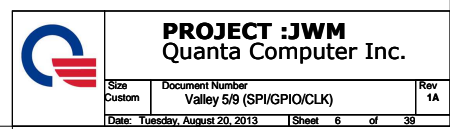
BOARD_ID[0:3] Model Name

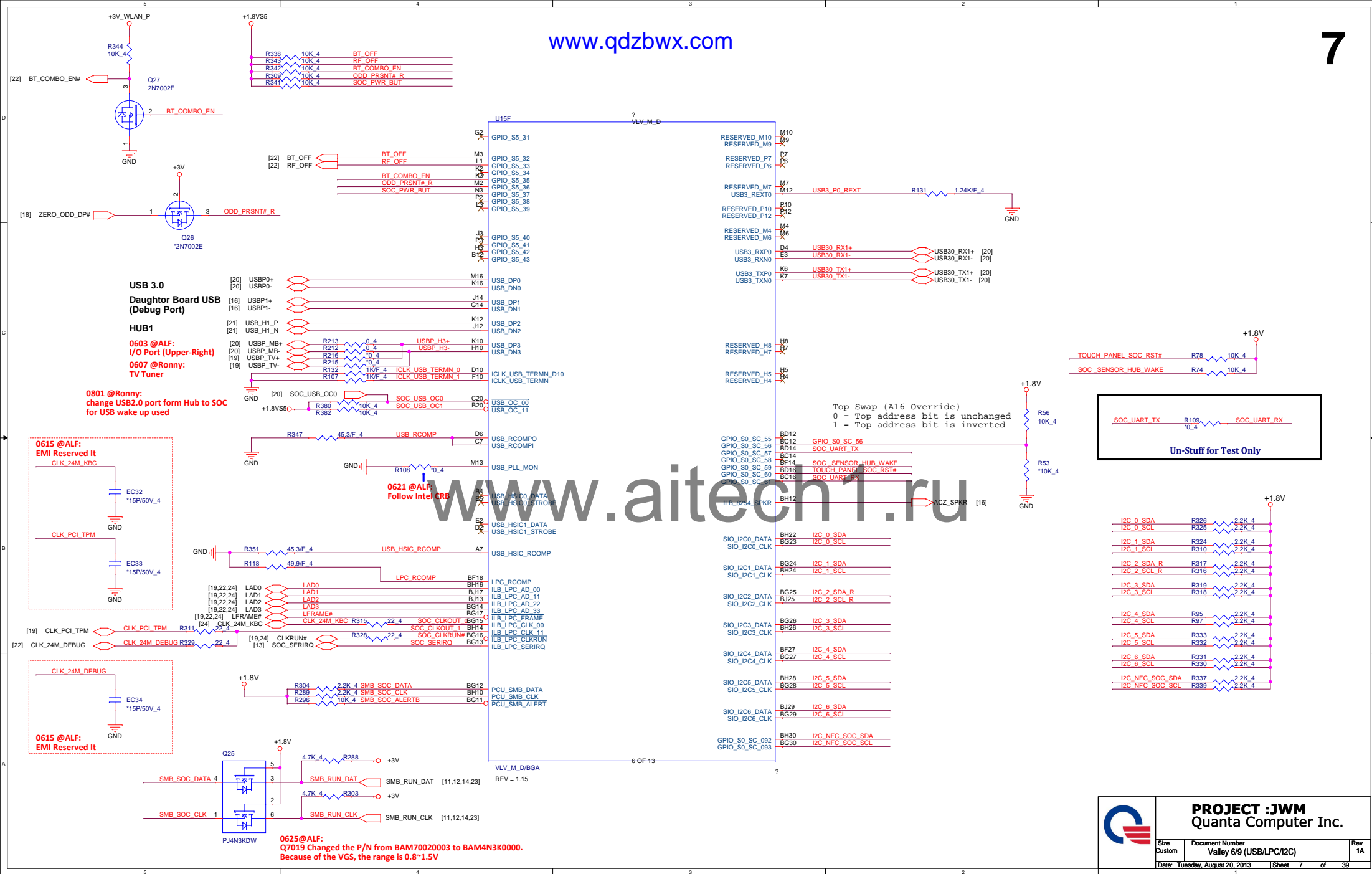
JWM	W08
0001	0000

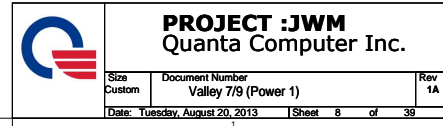


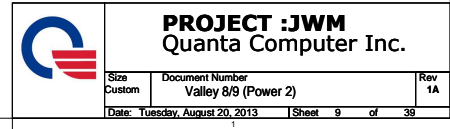
www.tech.ru

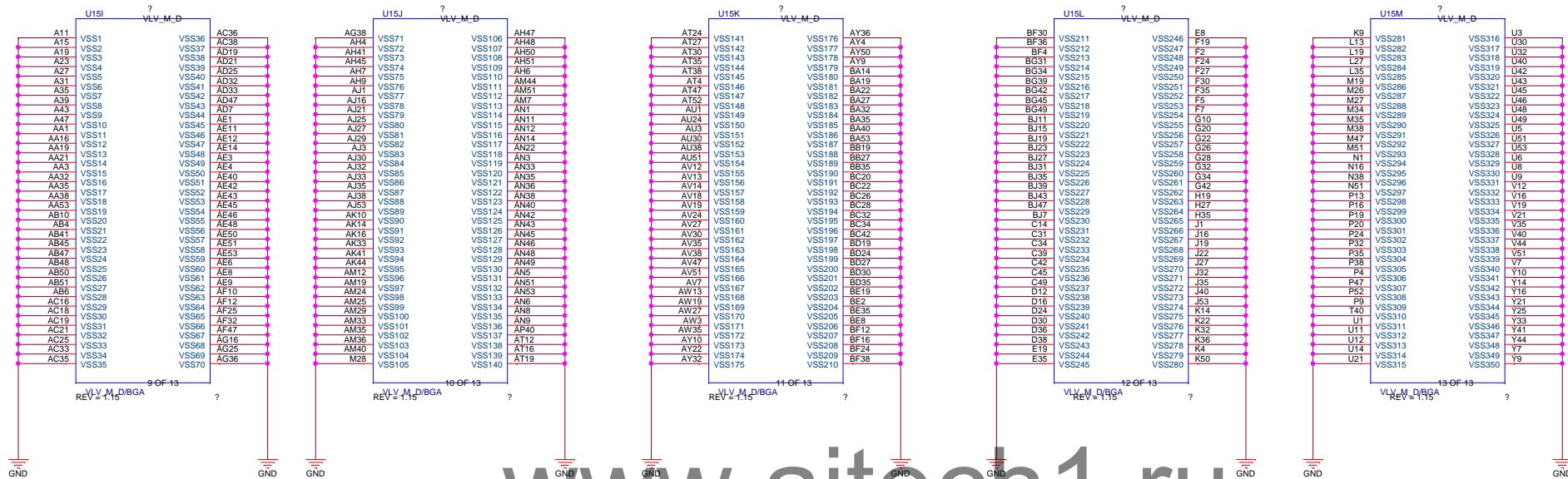






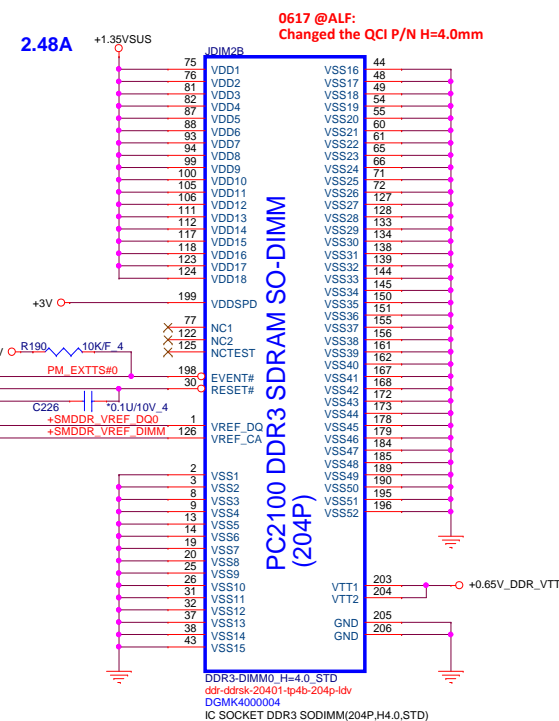
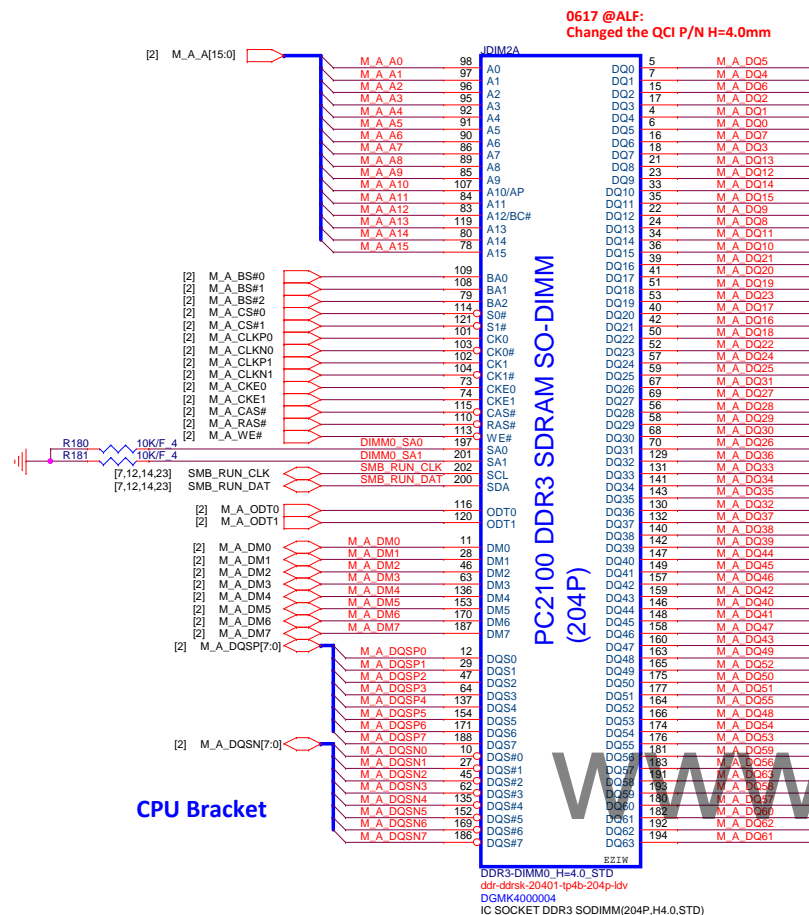






PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Valley 9/9 (GND)	1A
Date: Tuesday, August 20, 2013 1 Sheet 10 of 39		

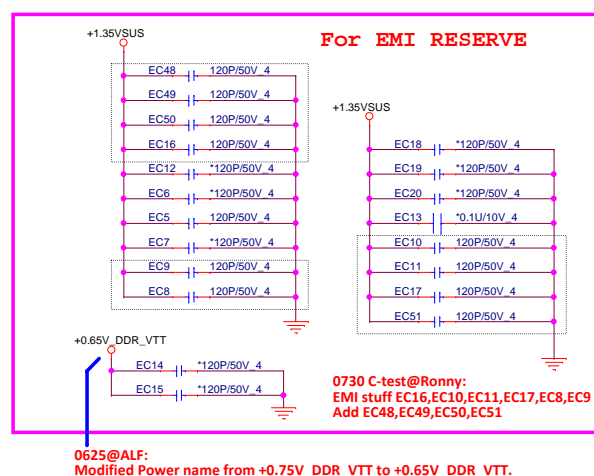


[5,7,9,12,13,14,15,16,17,18,19,20,21,22,23,24,25,35,37] +3V

[2,8,12,28,35] +1.35VSUS

[12,28] +0.65V_DDR_VTT

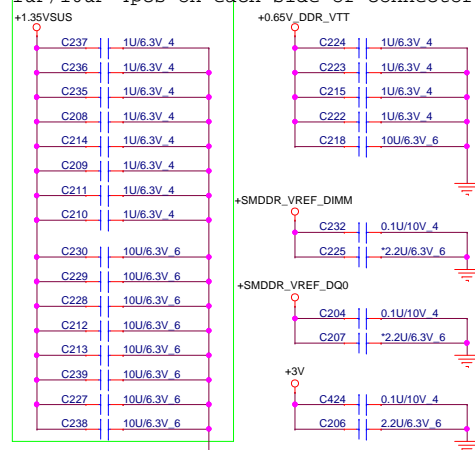
[11,12] +SMDDR_VREF_DIMM

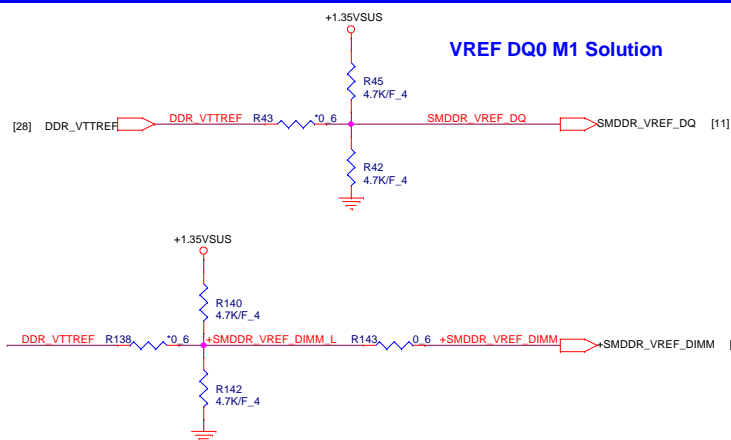
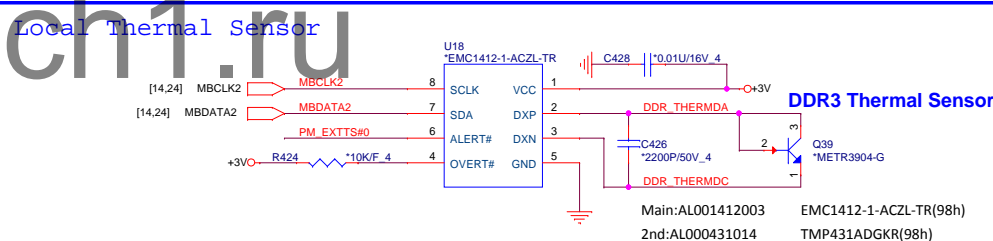
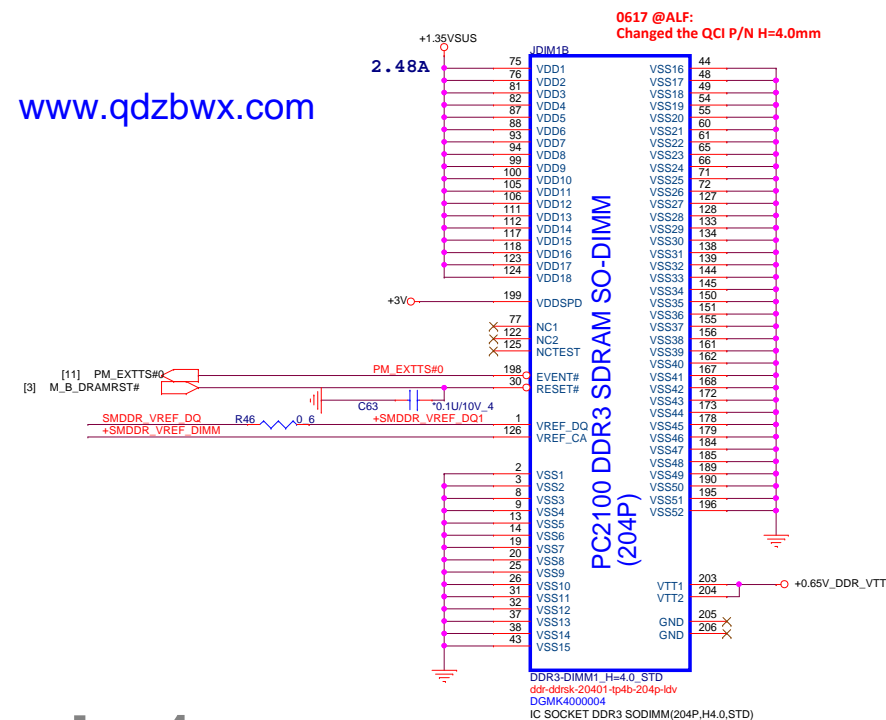
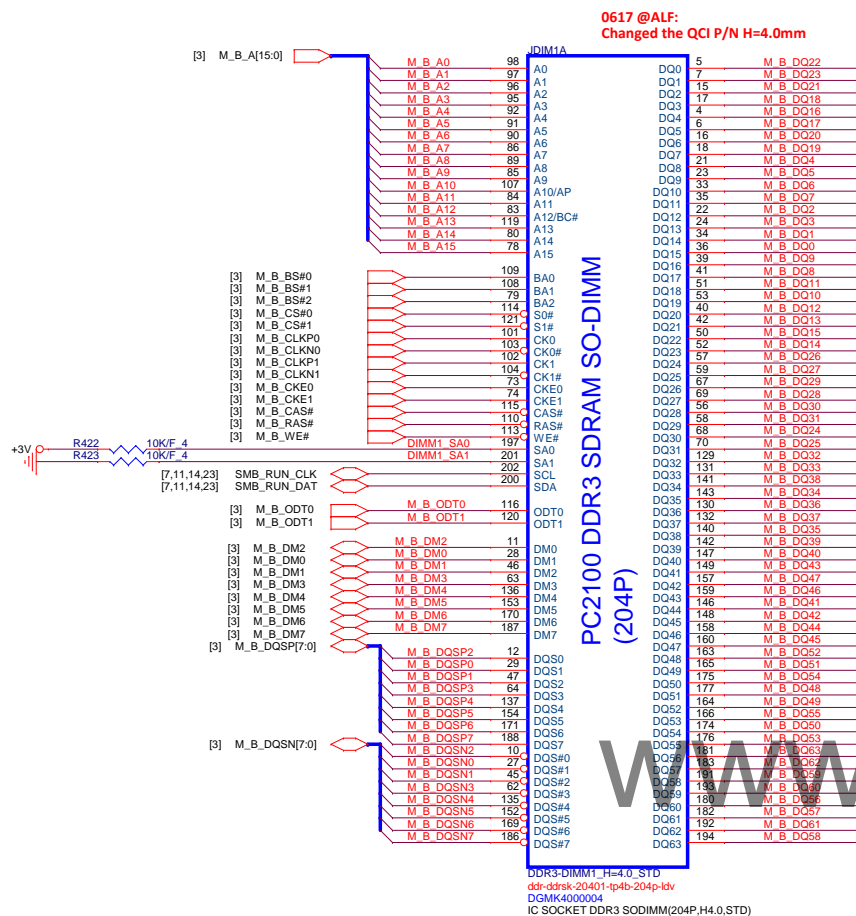


0625@ALF:
Modified Power name from +0.75V DDR VTT to +0.65V DDR VTT.

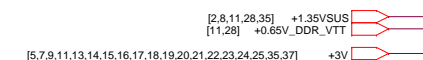
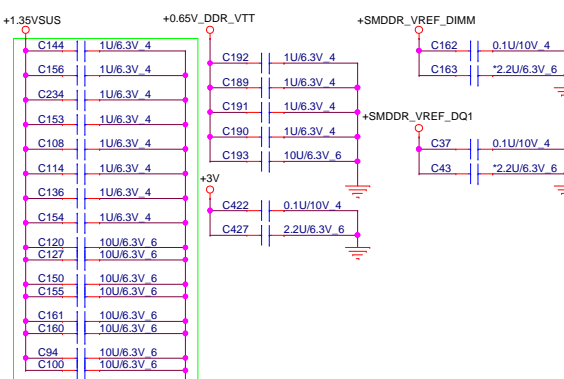
Place these Caps near So-Dimm0.

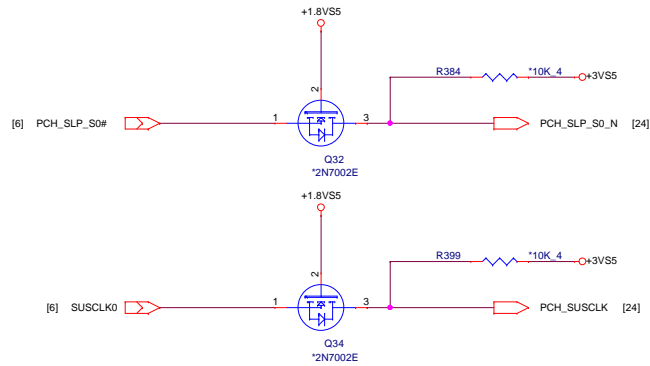
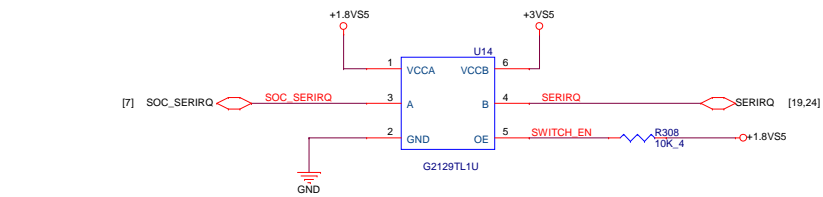
~~1uF/10uF 4pcs on each side of connector~~



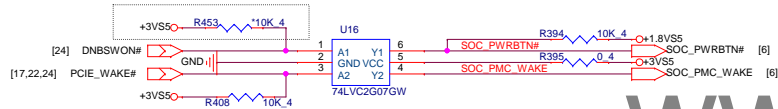


Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector

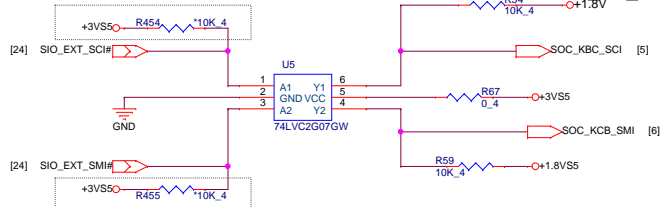




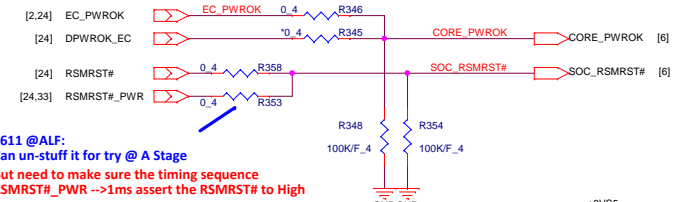
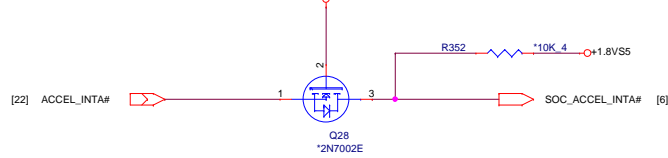
0801@Ronny
reserve Pull-up resistor R453



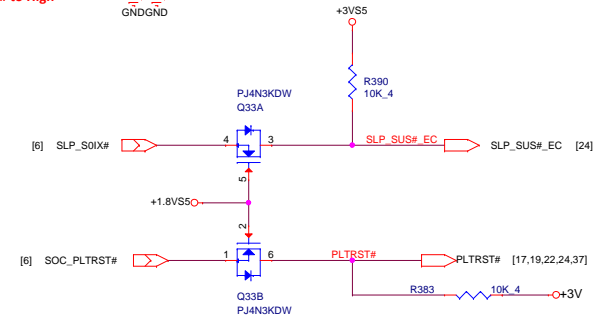
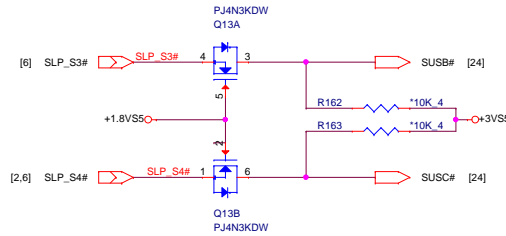
0801@Ronny
reserve Pull-up resistor R454



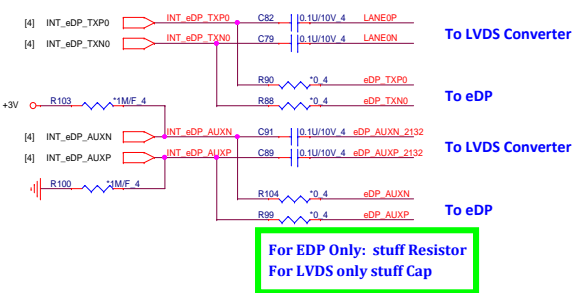
0801@Ronny
reserve Pull-up resistor R455



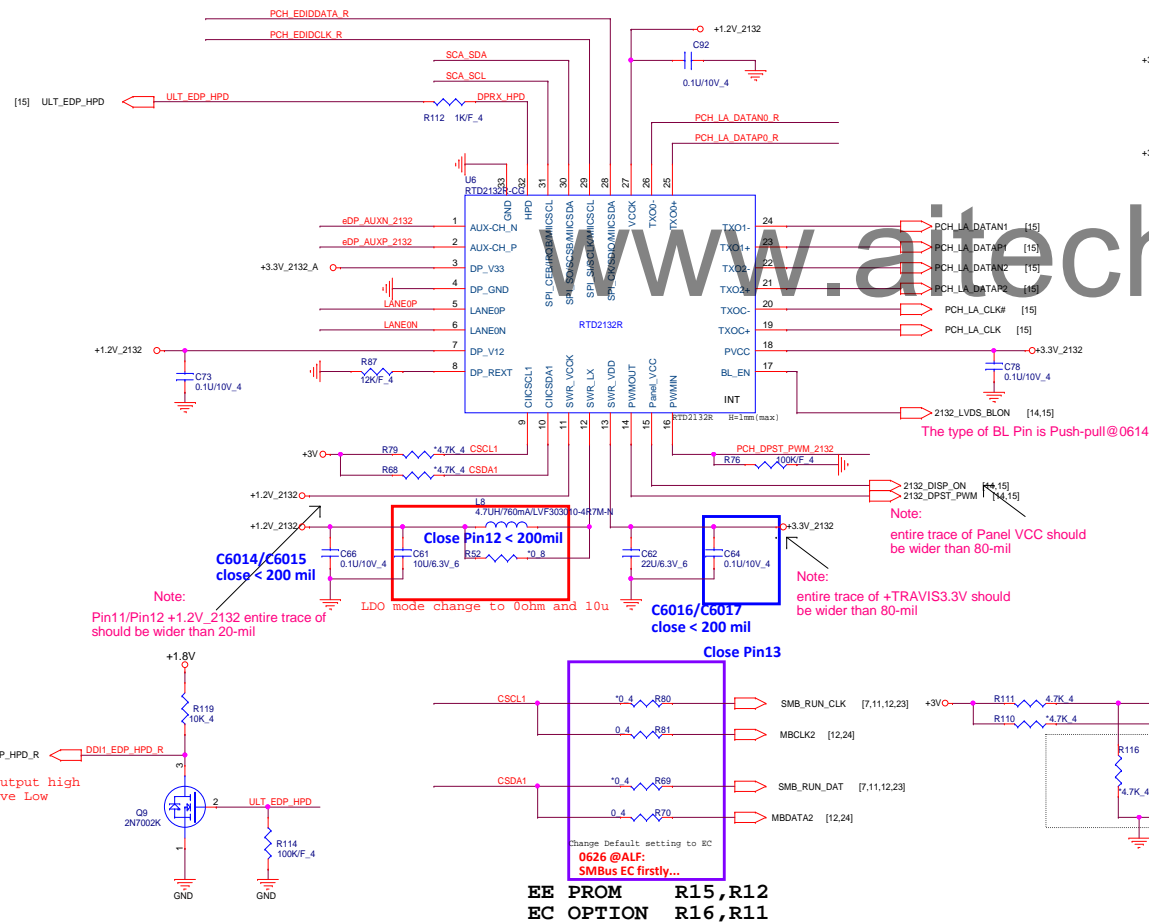
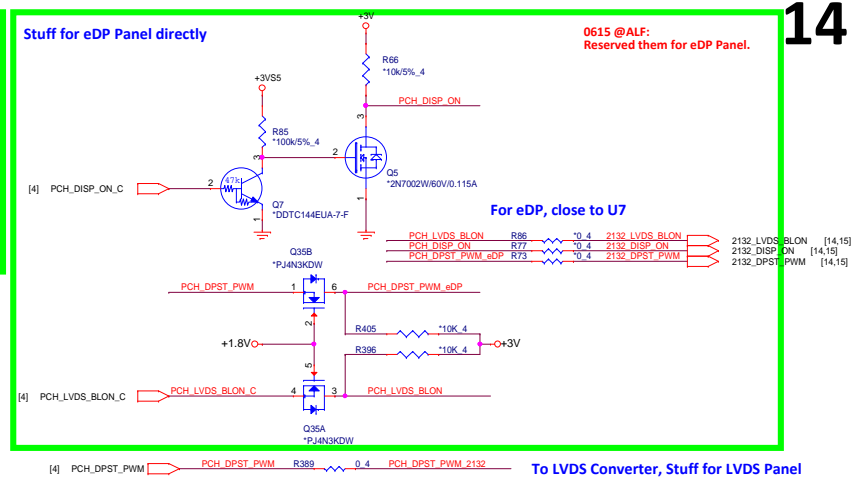
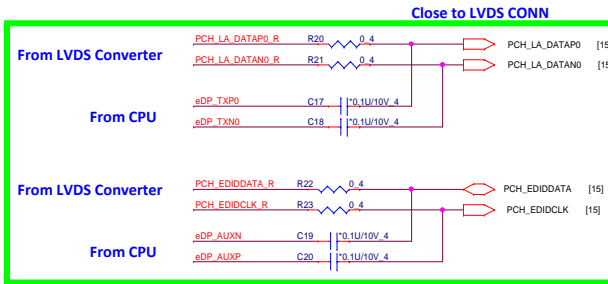
0611 @ALF:
Can un-stuff it for try @ A Stage
But need to make sure the timing sequence
RSMRST#_PWR -->1ms assert the RSMRST# to High



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www.qdzbwx.com

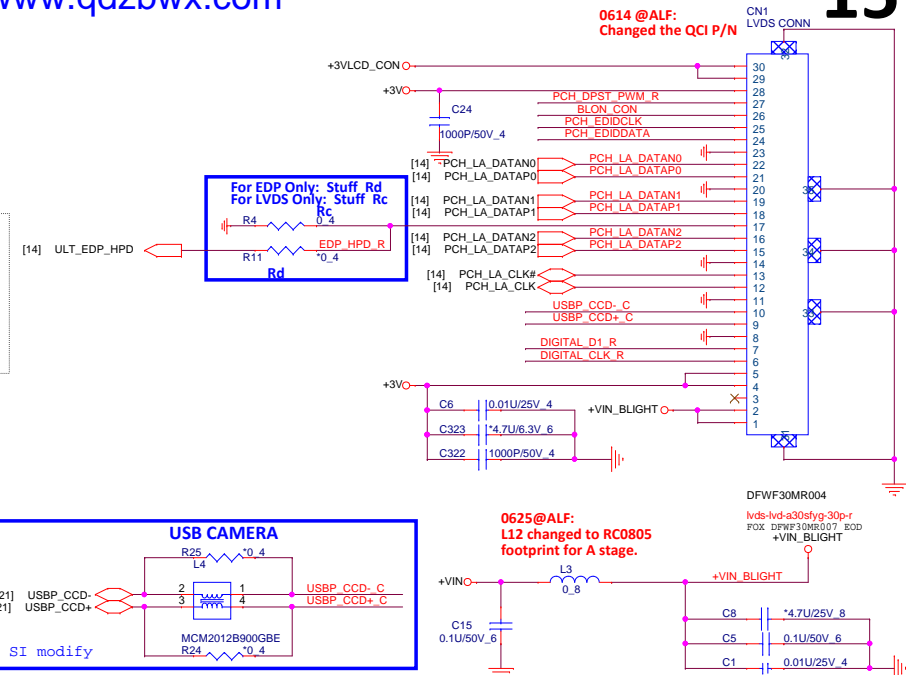


		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

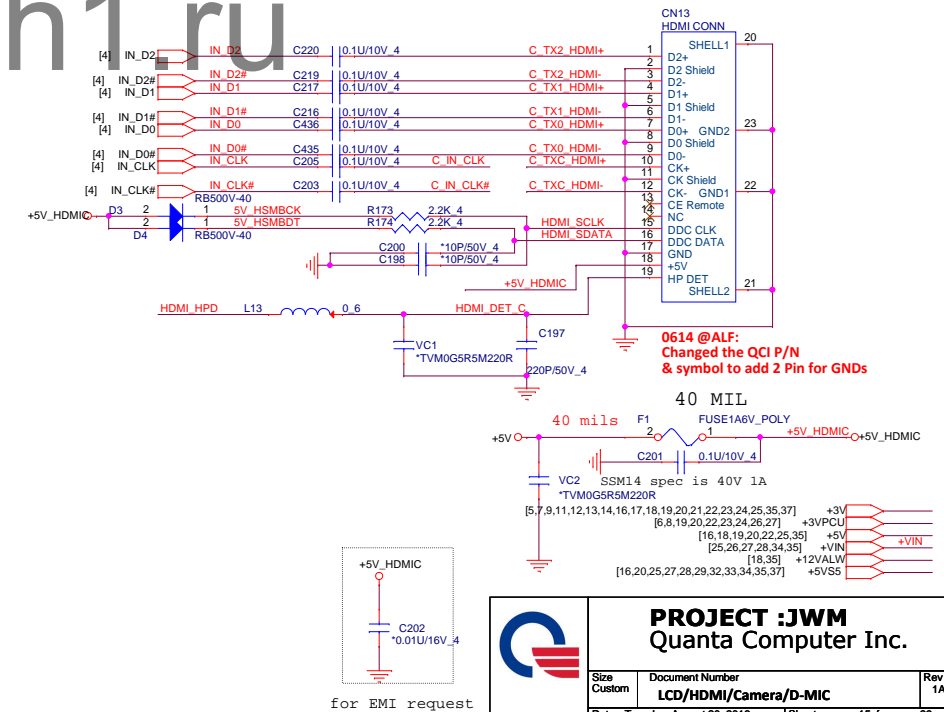
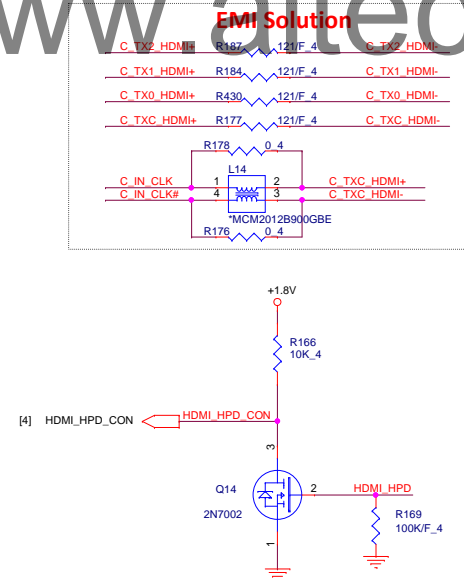


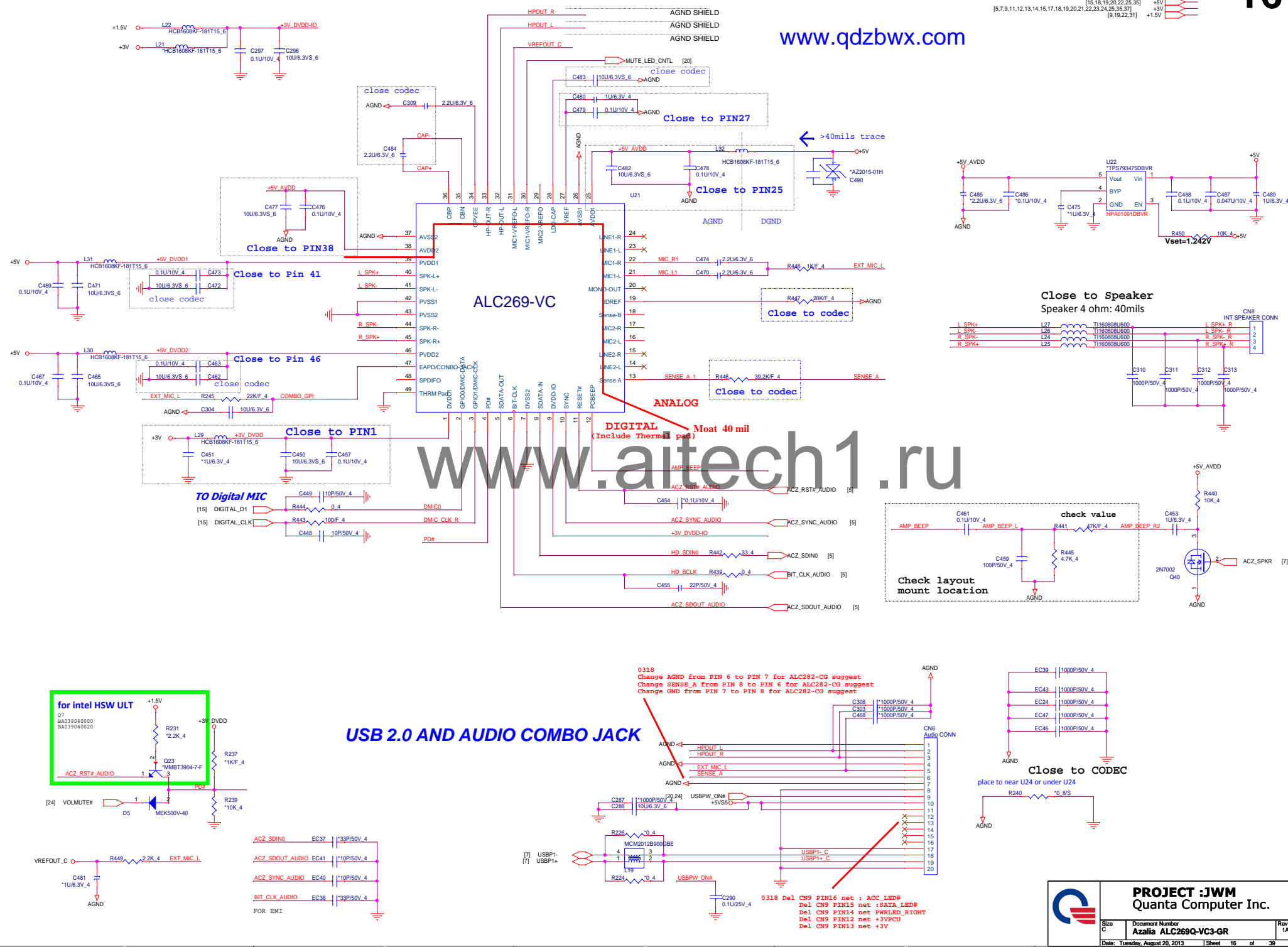
PROJECT :JWM
Quanta Computer Inc.

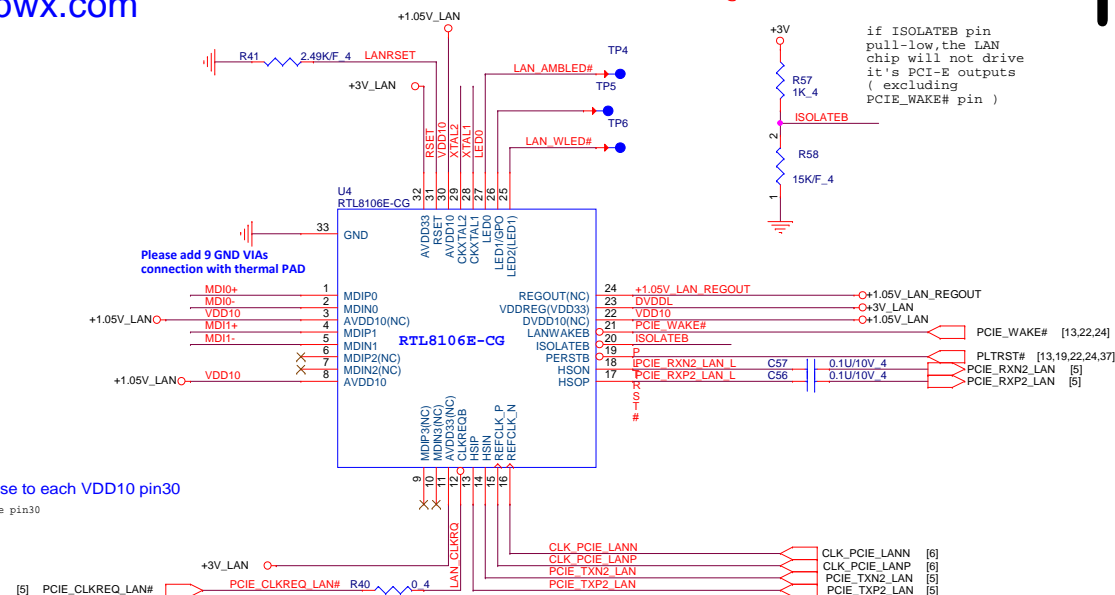
Size C Document Number
LVDS converter RTD2132R
Date: Tuesday, August 20, 2013 Sheet 14 of 39



EMI Solution

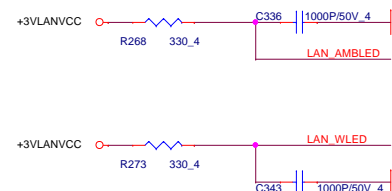


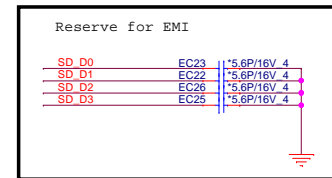
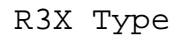




[5,7,9,11,12,13,14,15,16,18,19,20,21,22,23,24,25,35,37] +3V
[22,35] +3VLANVCC

The diagram illustrates the wiring for the RJ45 connector (CN1: RJ45_CONN) for the White and Amber LEDs. The connector has 12 pins. The White LED (LAN_WLED, LAN_WLED#, MDI1+, MDI1-, MDI0+, MDI0-) is connected to pins 1 through 8. The Amber LED (LAN_AMBLED, LAN_AMBLED#, LED_GRE_P, LED_GRE_N) is connected to pins 9 through 12. The circuit includes a 68P/50V_4 capacitor (C339) connected to ground. The White LED is connected to GND1 (pin 14) and GND (pin 13). The Amber LED is connected to GND1 (pin 14) and GND (pin 13).



Share Pin SD / MMC

SD WP SD D0 R R22 0.4 SD D0
SD D1 R R23 0.4 SD D1

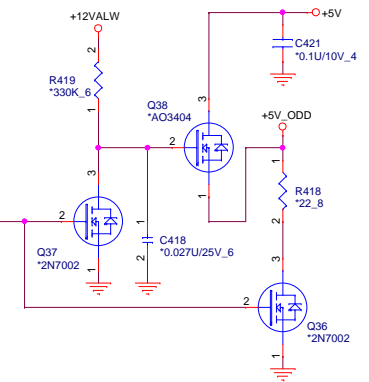
www.aitech1.ru

14" SATA ODD

Bypass CAP close conn



High : ODD power down
Low : ODD power on

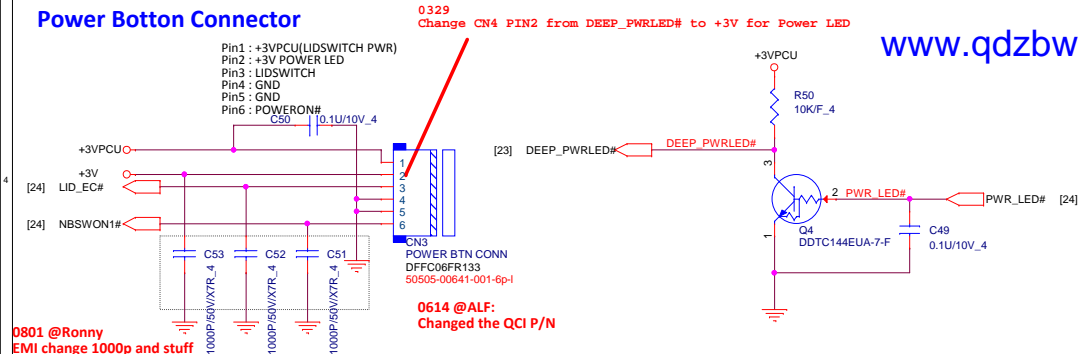


PROJECT :JWM
Quanta Computer Inc.

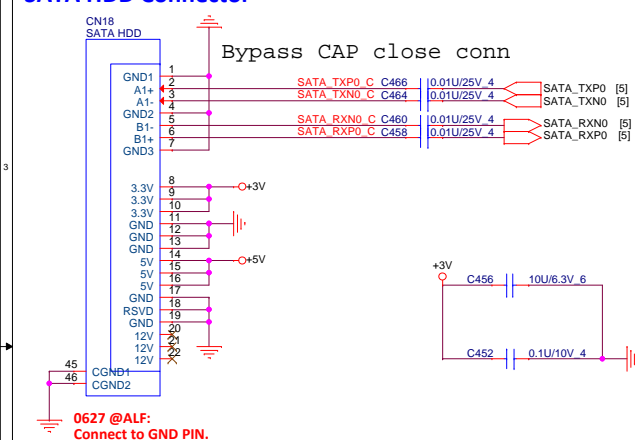
Size Custom	Document Number RTS5170-GRT&CR SOCKET	Rev 1A
Date: Tuesday, August 20, 2013		Sheet 18 of 39

Power Button Connector

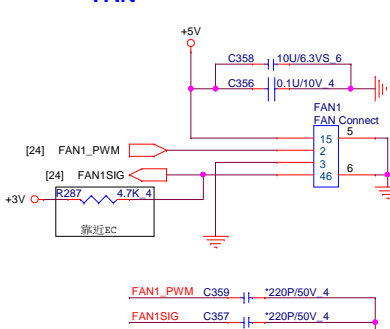
www.qdzbwx.com

0327 :
DEL Touch Pad Connector CN7 for U83

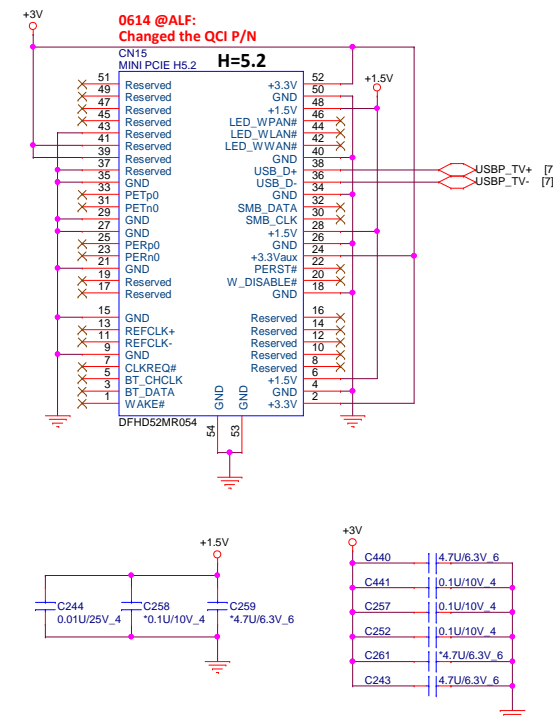
SATA HDD Connector



FAN



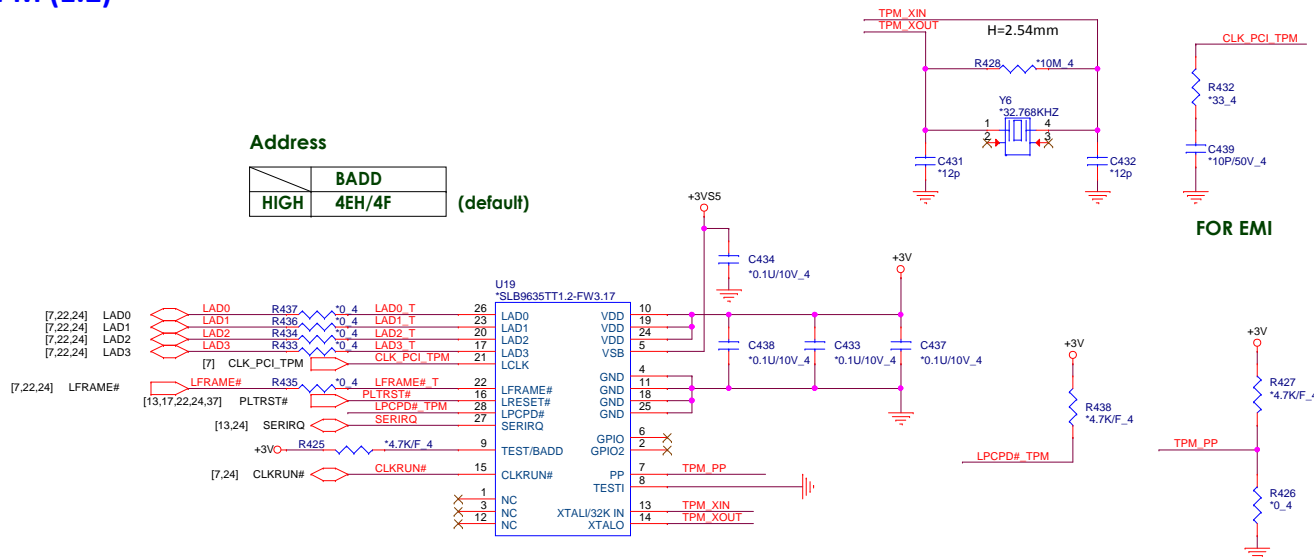
Mini PCI-E Card 2- Full size mSATA/TV Card



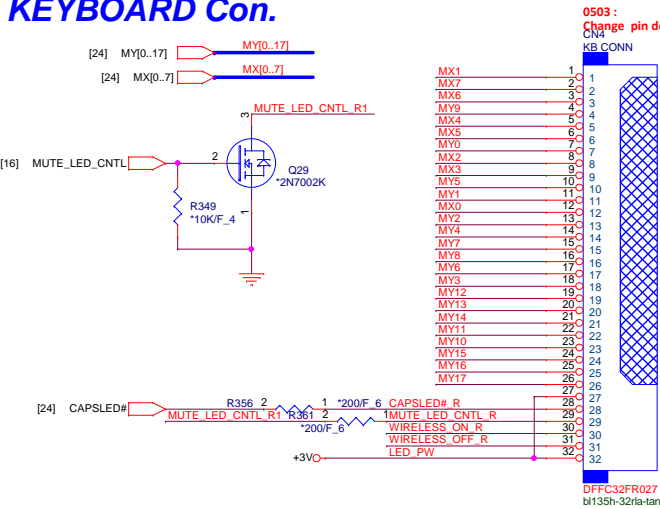
TPM (1.2)

Address

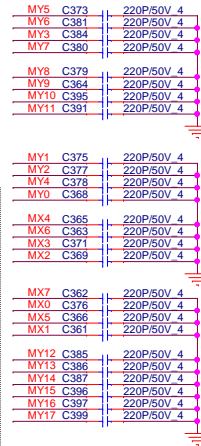
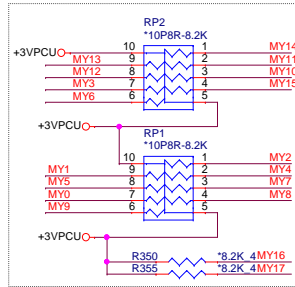
	BADD
HIGH	4EH/4F (default)



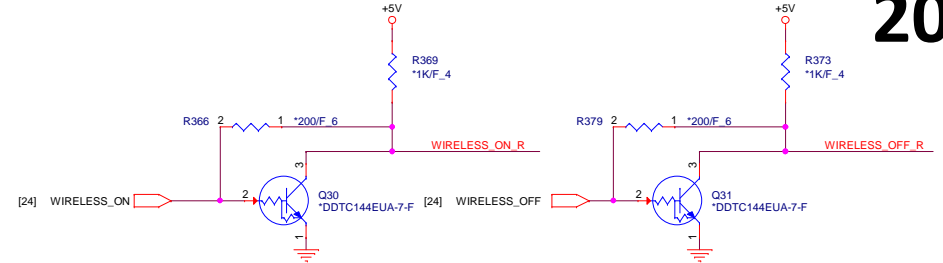
KEYBOARD Con.



KEYBOARD PULL-UP

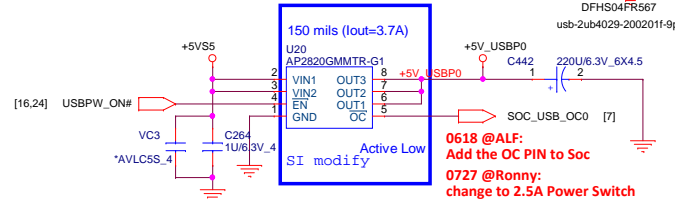
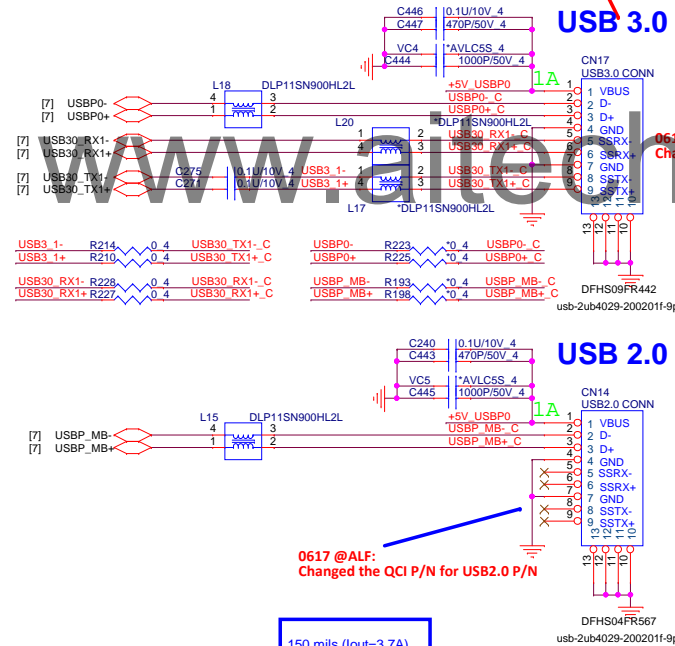
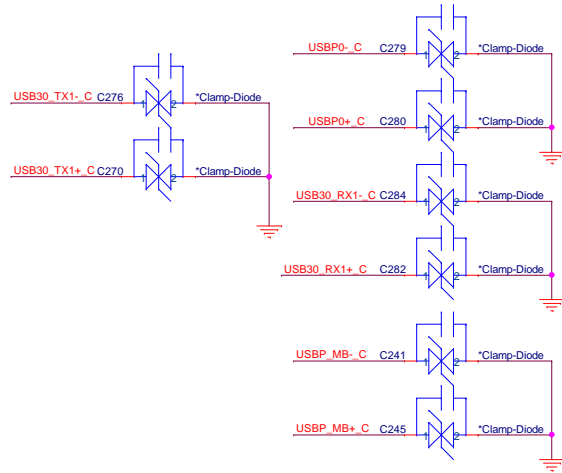


20



USB 2.0/3.0 Combo

0603 @ALF:
BTM only has one USB3.0 port, and define the CN20 (Bottom-left) at first



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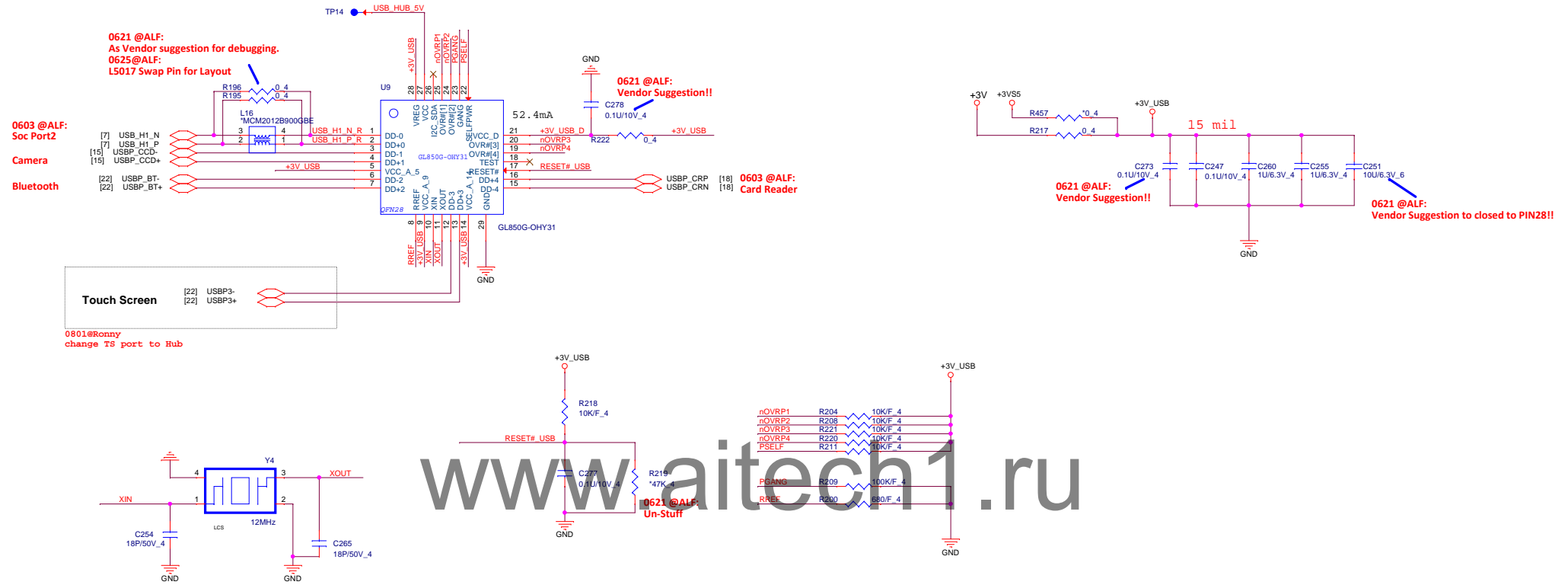


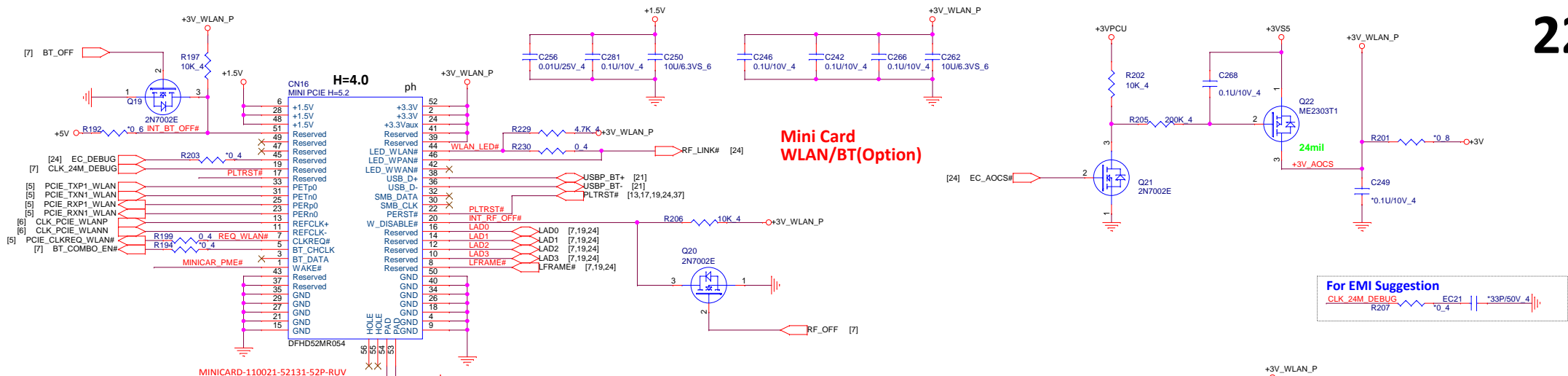
PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB3.0/KB	1A
Date: Tuesday, August 20, 2013	Sheet	20 of 39

[16,25,27,28,29,32,33,34,35,37]
[6,8,19,22,23,24,26,27]

+5V5S
+3VPCU



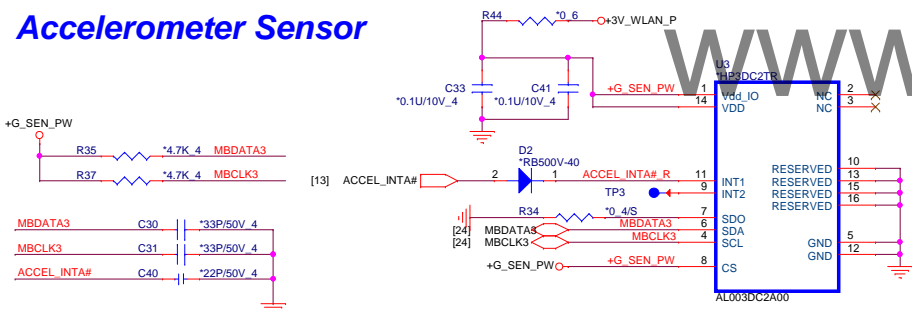


0614 @ALF:
 Changed the QCI P/N

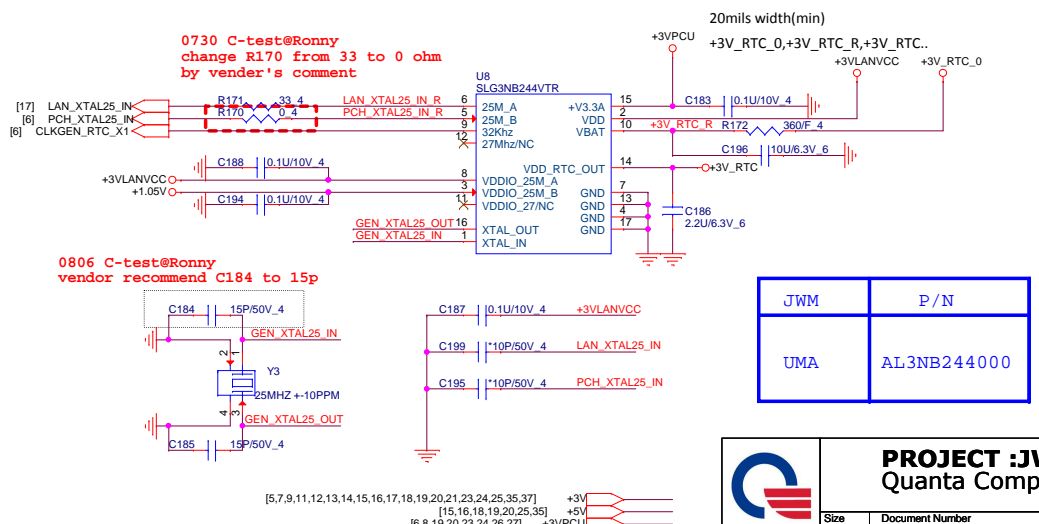
www.qdzbwx.com

Support Wake Function(Reserve)

Accelerometer Sensor

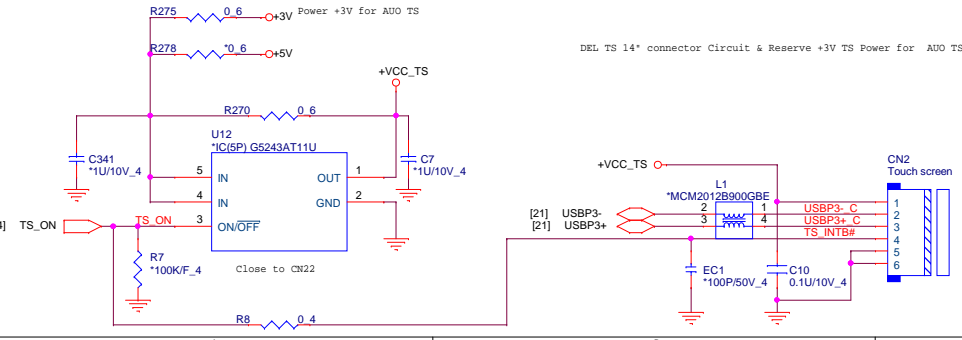


Green CLK Circuitry



JWM	P/N
UMA	AL3NB244000

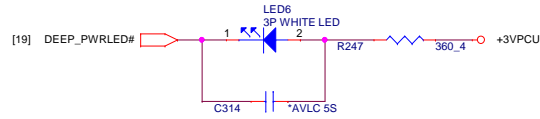
Touch screen



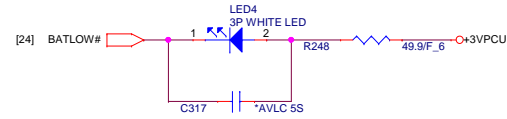
PROJECT :JWM Quanta Computer Inc.		
Size Custom	Document Number	Rev 1A
	WLAN/G-Sensor/G-CLK/TS	
Date: Tuesday, August 20, 2013	Sheet 22of 39	

LED Status

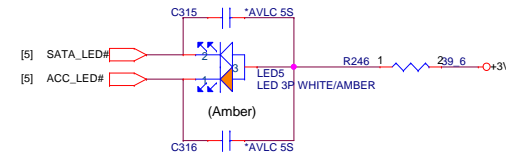
PWR LED



BAT LED



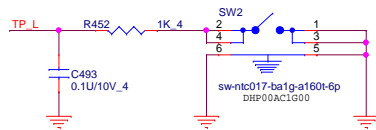
SATA LED



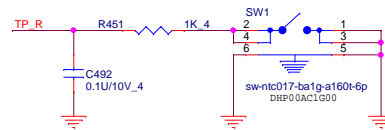
Function Button

0327 :
 ADD SW1/SW2/R14/R5/C14/C21 Function Button for JWU

Left



Right

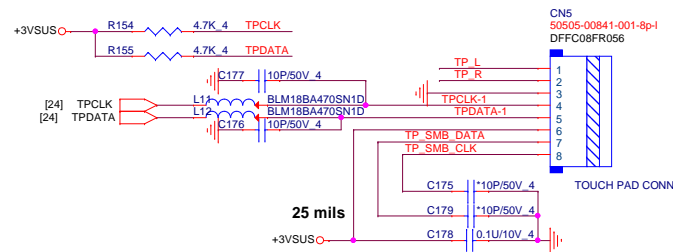
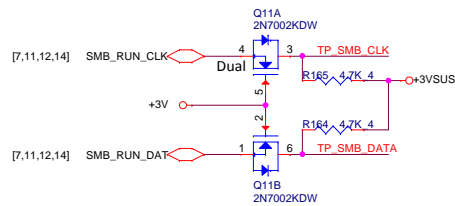


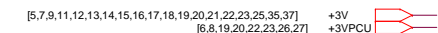
Touch Pad Connector

www.aitech1.ru

To Touch pad

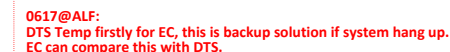
0327 :
 ADD Touch Pad Connector CN27 for JWU





0614 @ALF:
After meeting with NB5, reserved them first.
0617@ALF:
Delete all parts for CPU NTC thermal policy.

Layout Notes:
Closed to Soc, one is on TOP, other is on Left



Reserve for ENE Hold time issue

MBCLK2	C330	*10P/50V_4
MBDATA2	C333	*10P/50V_4
MBCLK	C327	*10P/50V_4
MBDATA	C329	*10P/50V_4
EC_GPURT_CLK	C334	*10P/50V_4
EC_GPURT_DATA	C337	*10P/50V_4

0615 @ALF:
EMI Suggestion to add 22ohm

BIOS_CS#
BIOS_SPI_CLK
BIOS_WR#
BIOS_RD#

U13
CE#
SCK
SI#
HOLD#
WP#
VSS

VDD
VSS

C347
0.1uF
VDD
VSS

8
7
4

R274
22
R272
22
R272
22
R279
10K
F_4

+3VPCU
R272
10K
F_4

SPI_3P_3
SPI_7P
10K
F_4

AK352N0V00
soic8-6_1_27-pm25010a

0615 @ALF:
Changed the SPI Winbond Part



PROJECT :JWM
Quanta Computer Inc.

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Screw Holes

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EMI 0626 @ALF:
EMI Suggestion for Power Shape

25

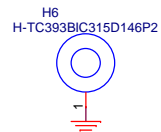
Stuff NUT Location:

0625 @ALF:
Added 2 pcs Holes for JWM Fan Module.



0701 @ALF:
Same as BM5, Stuff NUT on TOP side

FAN nut
Nut PN:MBFF4001010



0625 @ALF:
Modified the Hole's FP.

0729 @ALF:
change to BOT side

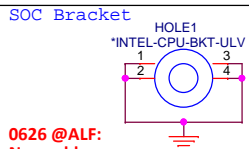
Mini-PCie Nut for TV Card
Nut PN:MBZR7001010



0625 @ALF:
Modified the Hole's FP.

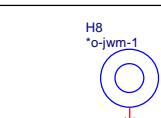
0729 @Ronny:
delete Hole

SoC Bracket



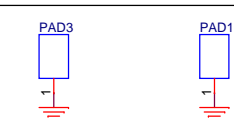
0626 @ALF:
New add

PCB Fan Hole (Internal)



0626 @ALF:
Modified the Hole's FP.

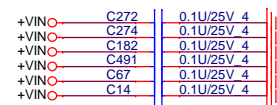
GND PAD



0729 : ADD PAD3
0805 : remove PAD2

+VIN Shape on SVCC Layer

0.1uF Caps * 6pcs

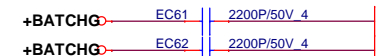
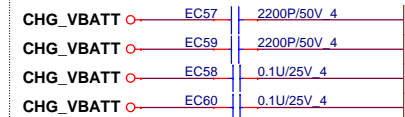
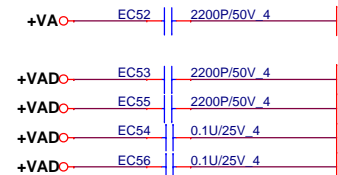


+VCC_GFX Shape on SVCC Layer

1000PF Caps * 2pcs

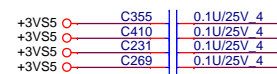


0731@Ronny: EMI add cap at Power source side



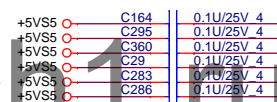
+3VS5 Shape on SVCC Layer

0.1uF Caps * 4pcs



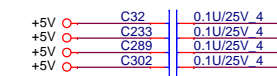
+5VS5 Shape on SVCC Layer

0.1uF Caps * 6pcs



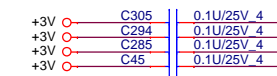
+5V Shape on SVCC Layer

0.1uF Caps * 4pcs



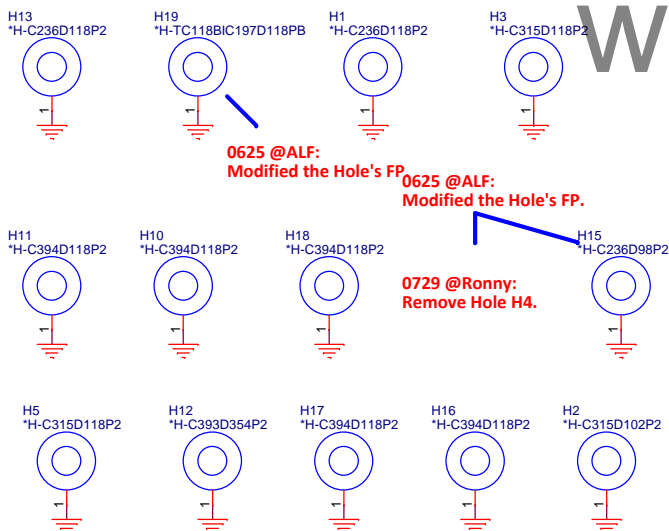
+3V Shape on SVCC Layer

0.1uF Caps * 4pcs



0329 :
ADD H35,H36,H37,PAD1 HOLE


0402 :
ADD H38 HOLE

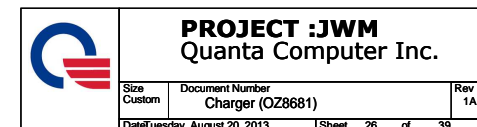


0625 @ALF:
Modified the Hole's FP.

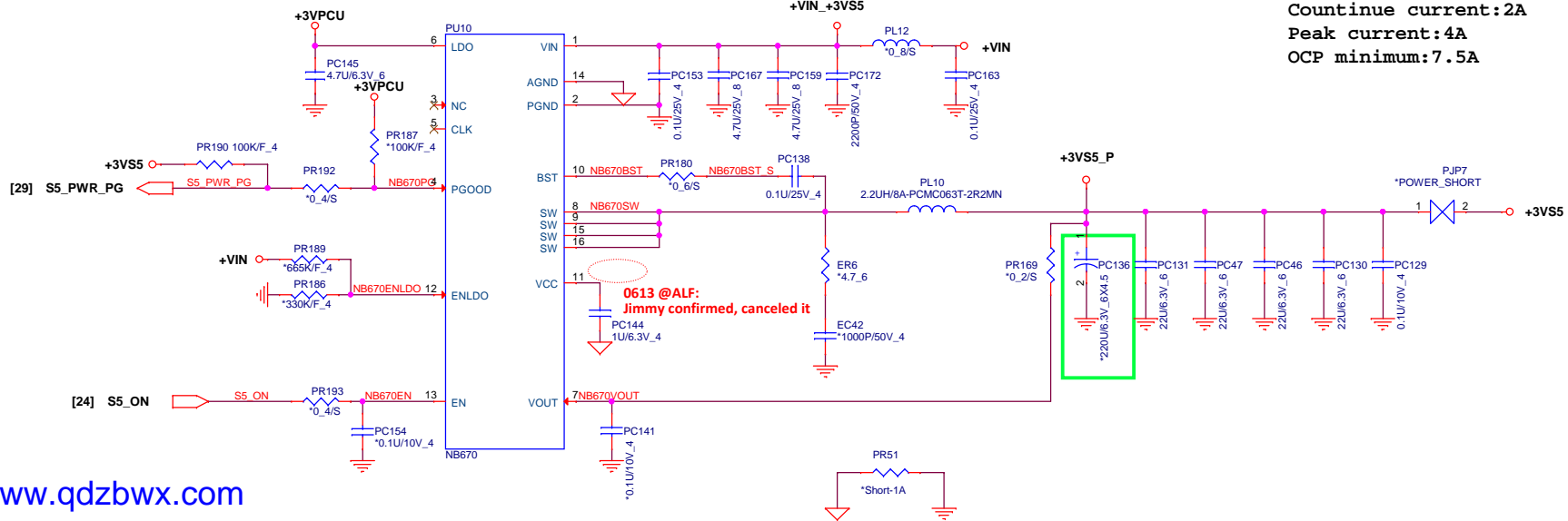
0625 @ALF:
Modified the Hole's FP.

0729 @Ronny:
Remove Hole H4.

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+3.3 Volt +/- 5%
 Countinue current:2A
 Peak current:4A
 OCP minimum:7.5A

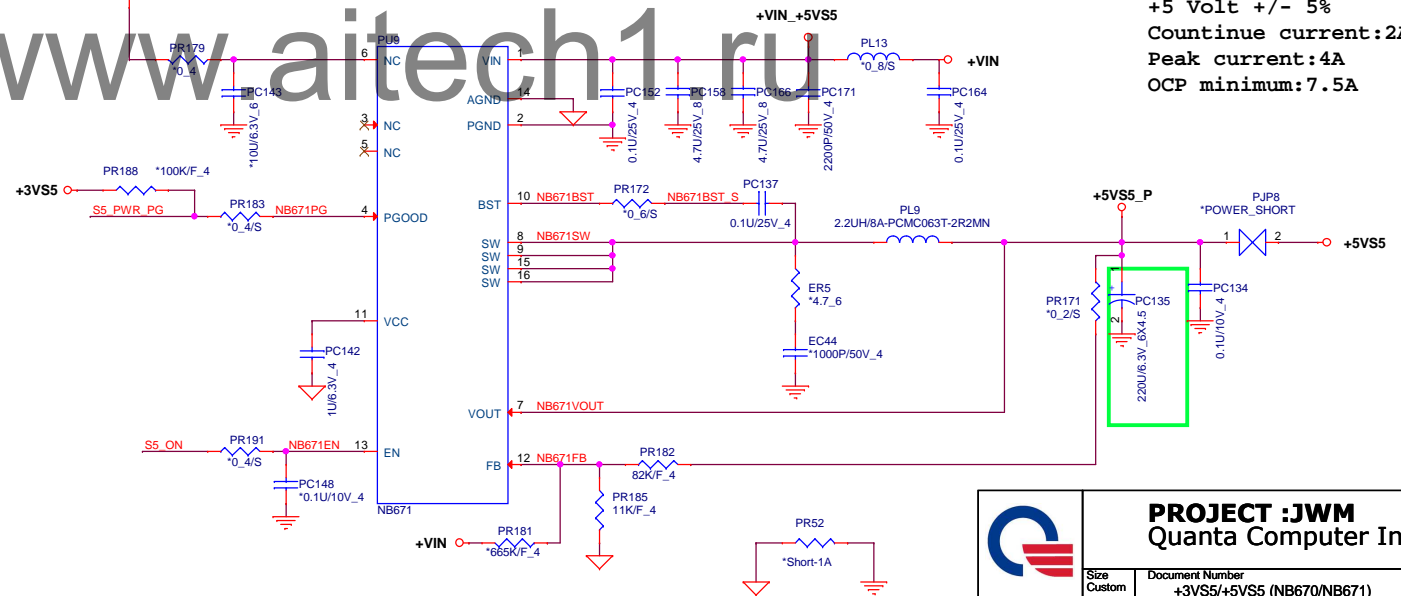


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0613 @ ALF:
 Aftered Power Jimmy confirmed, it is no need.

0611 @ ALF:
 Should be canceled, because has discharge IC.

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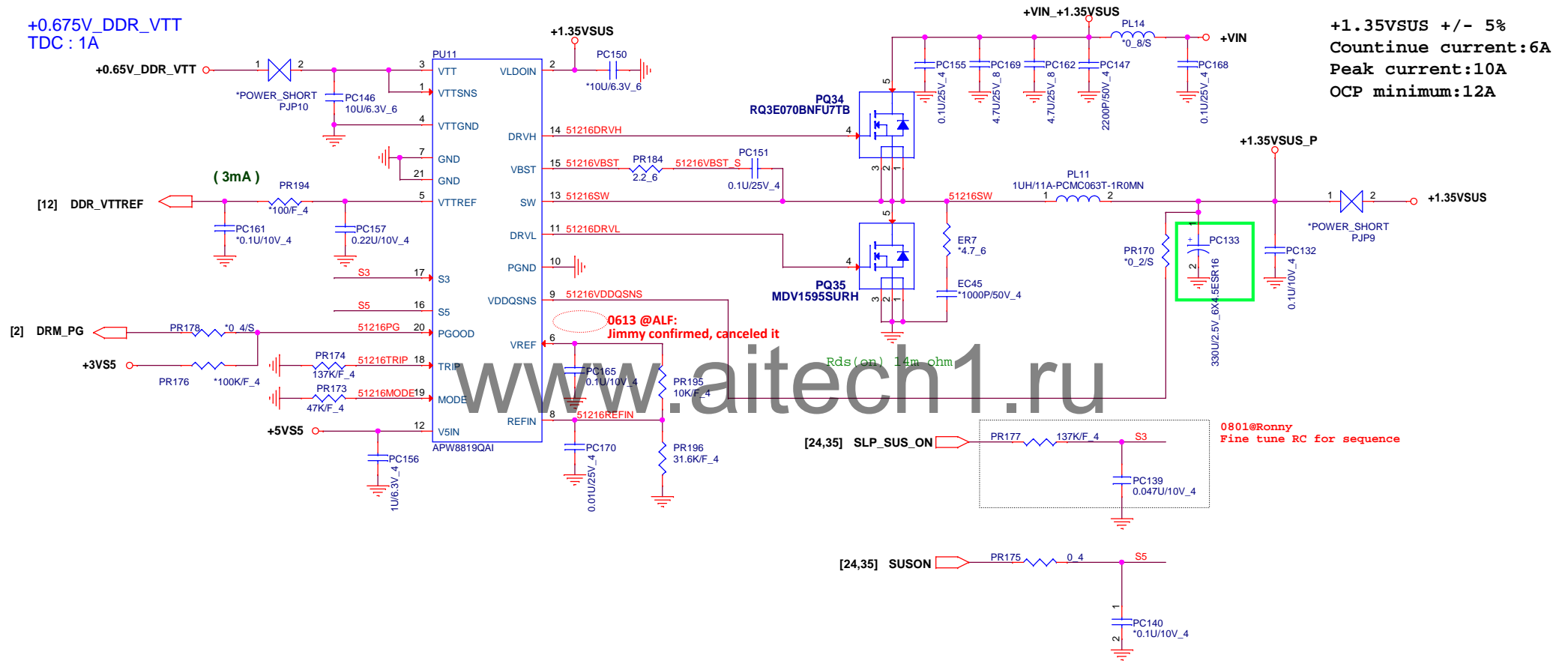


+5 Volt +/- 5%
 Countinue current:2A
 Peak current:4A
 OCP minimum:7.5A



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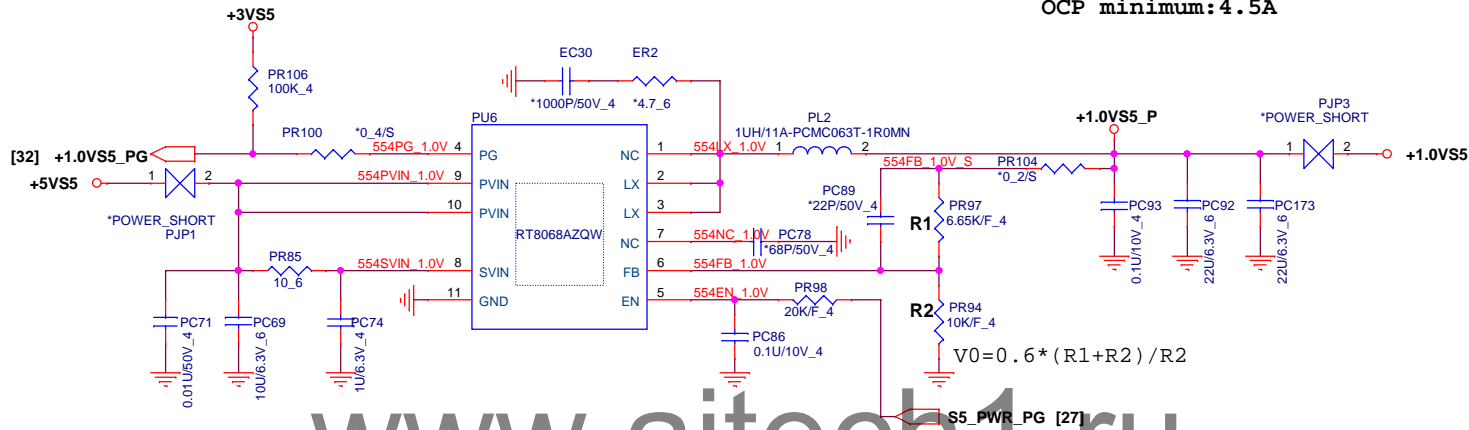
Size	Document Number	Rev
Custom	+3VS5/+5VS5 (NB670/NB671)	1A
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B	1.35/0.675V(TPS51216RUKR)	1A
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+1.0V_ALW Volt +/- 5%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4.5A



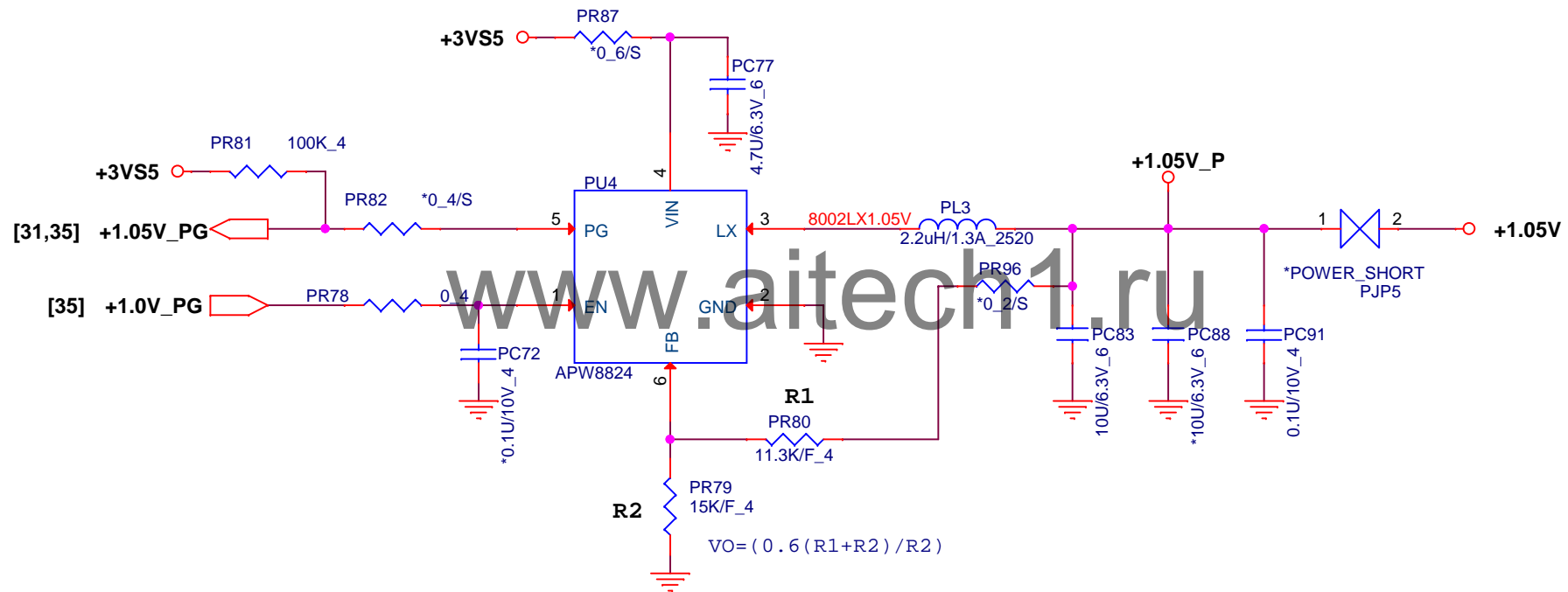
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Size	Document Number	Rev
B	+1.0VS5(APW8804)	1A
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+1.05V Volt +/- 5%
 Countinue current:1A
 Peak current:1.0A
 OCP minimum:2A



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Size
A

Document Number
+1.05V (APW8824)

Rev
1A

Date Tuesday, August 20, 2013

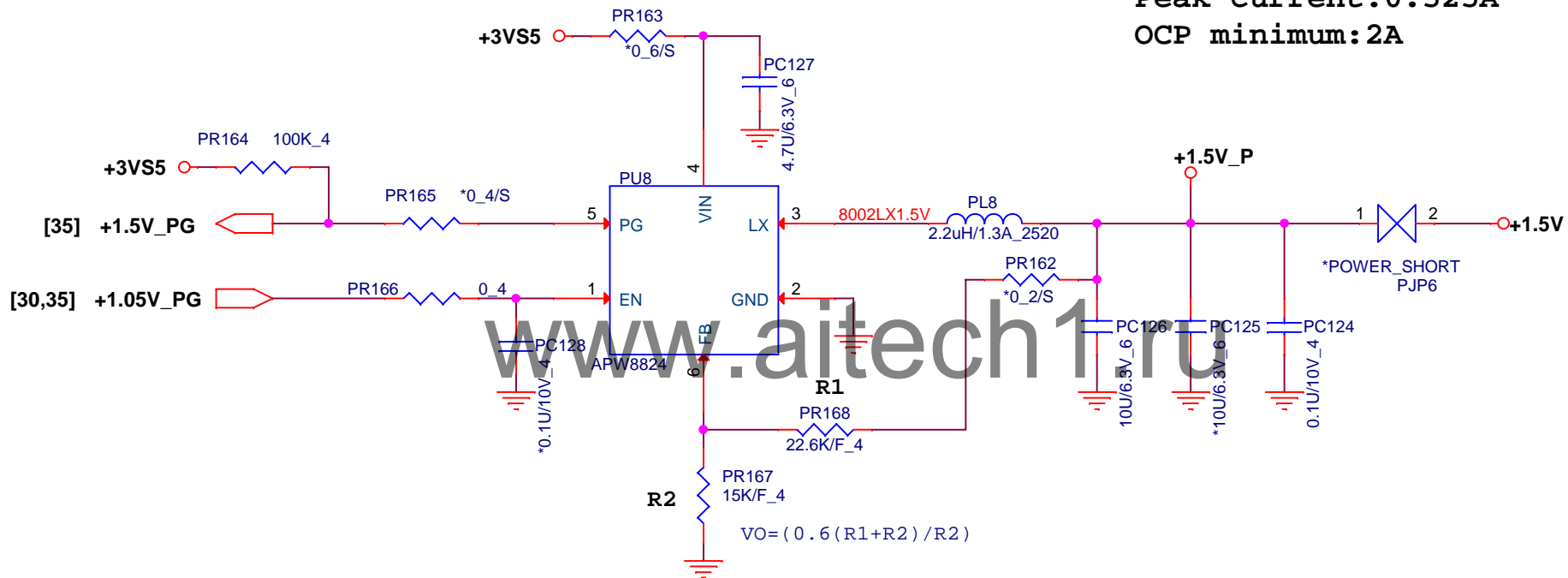
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+1.5V +/- 5%

Continue current: 0.45A

Peak current: 0.525A

OCP minimum: 2A



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Size
A

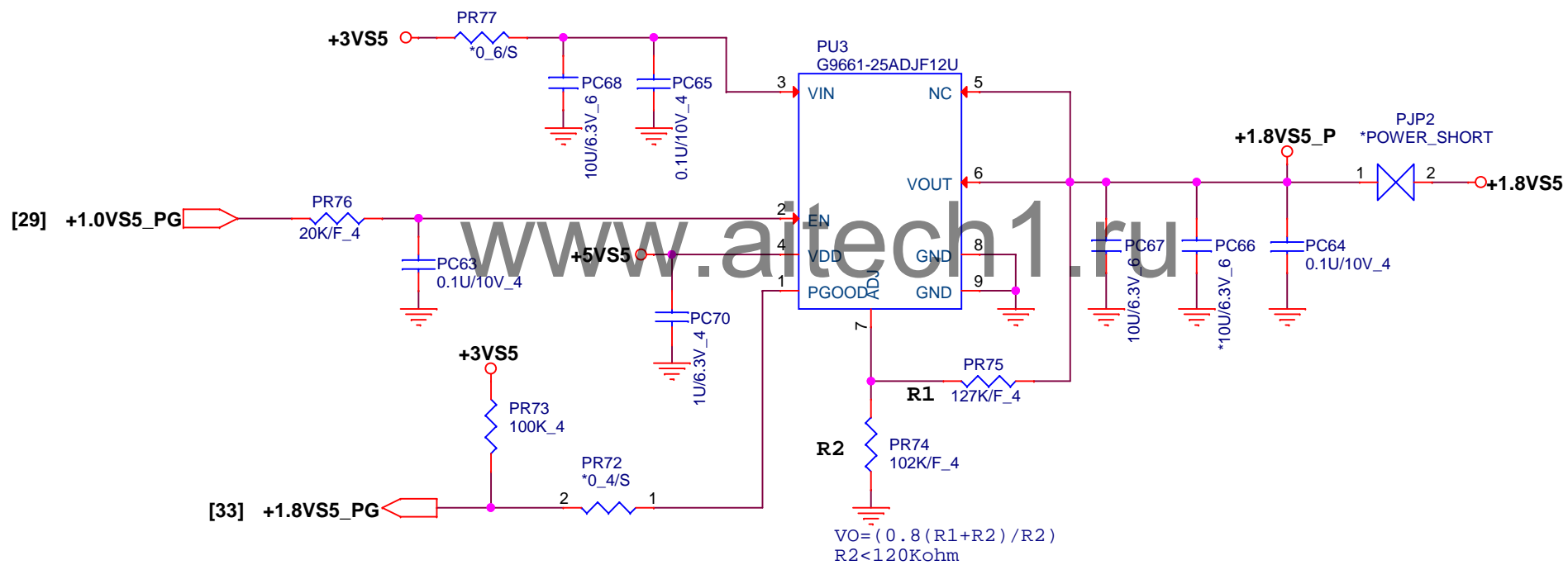
Document Number
+1.5V (APW8824)

Rev
1A

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+1.8V Volt +/- 5%
Countinue current:0.105A
Peak current:0.3A



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+1.2V Power Supply

Peak Current: 0.5A

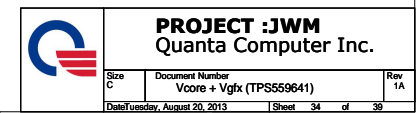
VO = (0.8 * (R1 + R2)) / R2
R2 < 120Kohm

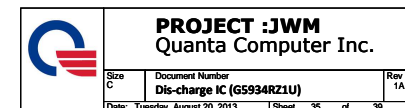
0626 @Power:
+1.24V Output.

Size
A

Rev	1A
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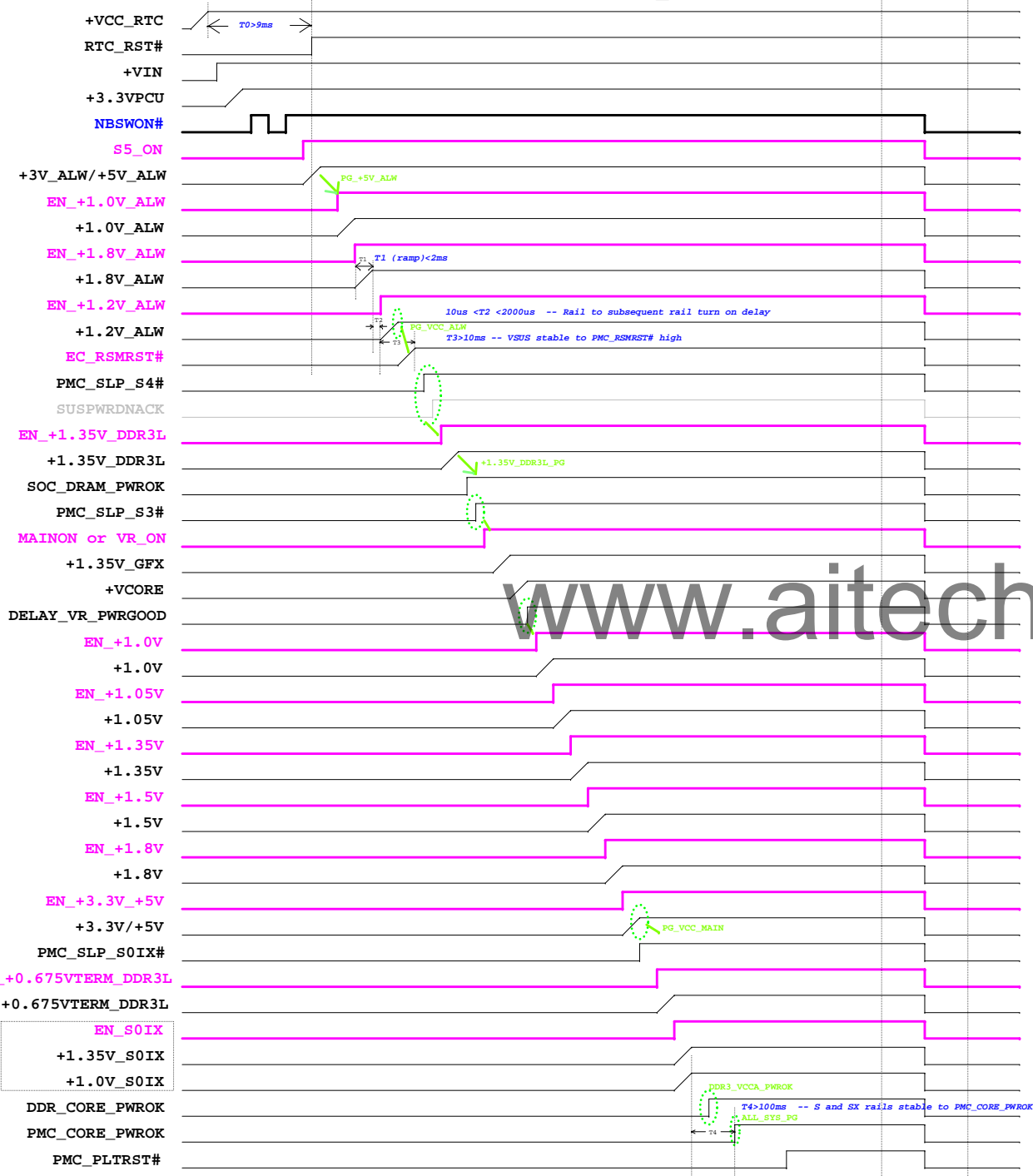
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Power on sequence OFF

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T0: +RTCVCC stable to RTCRST# high > 9ms
 T1: VR ramp up time from 10% to 90% voltage level < 2ms
 T2: Rail to subsequent rail turn on delay < 2ms
 T3: +VALWAS stable to EC_RSMRST# high > 10us
 T4: +VS rails stable to PMC_CORE_PWROK > TBD

NOTE:

1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

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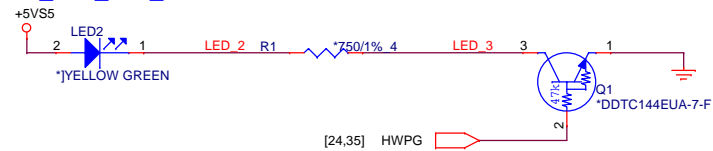
www.aitech1.ru

Green signals (PG) to EC
 Blue timing -- Intel
 Pink signals from EC

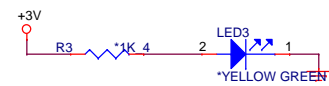
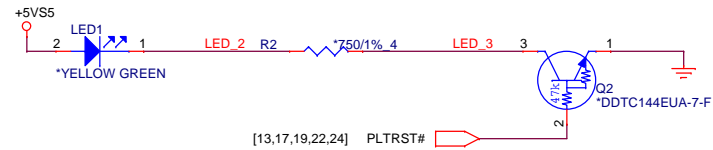
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LED For bring-up

EC_ALL_SYS_PG LED



PLTRST# LED

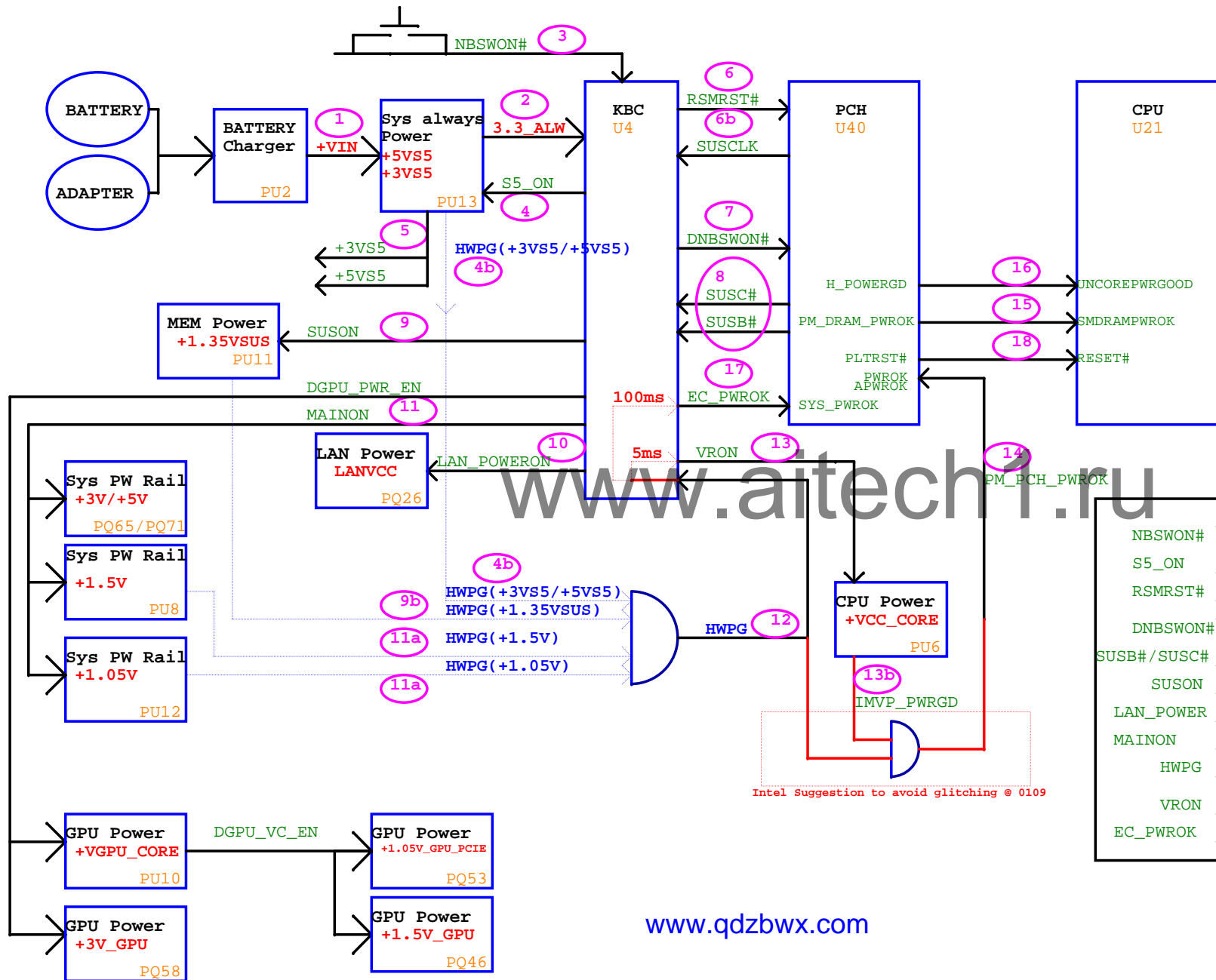


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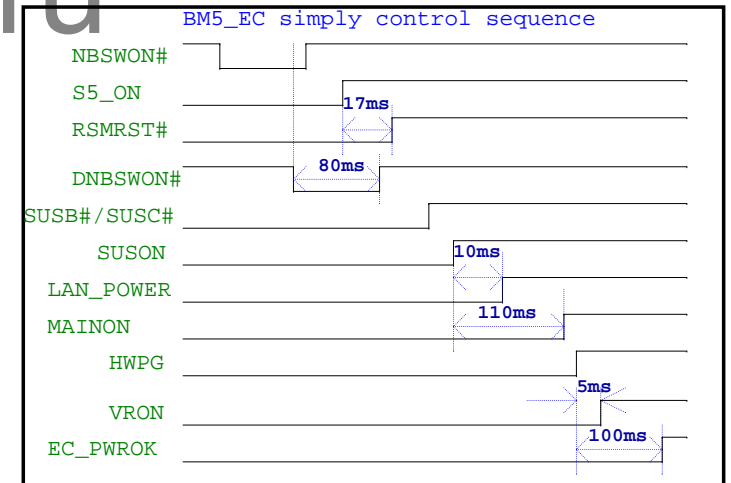


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Intel Suggestion to avoid glitching @ 0109

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